High-*k* Organic, Inorganic, and Hybrid Dielectrics for Low-Voltage Organic Field-Effect Transistors

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1. Introduction

The search for high dielectric constant (high-*k*) gate dielectric materials for field-effect transistor-enabled (FET) applications has stimulated important research activities in both conventional and unconventional electronics. Although it is not the focus of this Review Article, high-*k* dielectric technology is tremendously important in the well-established silicon electronics industry. Indeed, the continuous drive to increase integrated circuit performance through shrinkage of the circuit elements requires the Si transistor dimensions to be scaled down according to the well-known Moore's law.[1]

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Historically, this goal has been achieved by developing new optical lithography tools, photoresist materials, and critical dimension etch processes. However, it is now clear that, despite advances in these crucial process technologies, device performance in scaled devices will be compromised because the traditional materials used for transistor and capacitor fabrication (silicon and silicon dioxide) have reached their fundamental material limits.[2] Therefore, continuing scaling will require the introduction of new materials.[3] One of the key materials challenges, which if not addressed could interrupt the historical Moore's law progression, is the replacement of the silicon dioxide layer with new gate dielectric materials.[4] Despite a number of excellent properties, SiO_2 suffers from a relatively low dielectric constant ($k = 3.9$). Because high gate dielectric capacitance is necessary to enable the required drive currents for submicrometer devices and because capacitance for a film is proportional to k and inversely proportional to gate dielectric thickness (d), the SiO_2 layer thickness must be reduced accordingly to scaled device dimensions. Because of the large band gap of SiO_2 (~9 eV) and low density of traps and defects in the bulk, the leakage current through the dielectric layer is normally very low. However, for ultrathin SiO_2 films this is no longer the case.[5] When the physical thickness between the gate electrode and doped Si substrate becomes thinner than ~2 nm, according to fundamental quantum mechanical laws, the tunneling current increases exponentially with

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decreasing oxide thickness and dominates the leakage current. For silicon dioxide-based capacitors, the leakage current at 1 V increases from $\sim 10^{-5}$ to ~ 10 A/cm^2 when the dielectric layer thickness decreases from ~ 3 to ~ 1.5 nm, which is a $10^7\times$ current increase for a thickness change of only $2\times$.[6,7] These high leakage currents will invariably compromise the device performance as well as dissipate large amounts of power. It is therefore obvious that SiO_2 as deposited with current methods will very soon reach its limit as a gate dielectric for all kinds of low power applications. Although higher power dissipation may be tolerable with some high-performance processors, it quickly leads to problems for mobile devices. Eventually, another major limitation for thin oxides may come from their reduced lifetimes. In addition, the increased operation temperatures considerably increase the gate leakage through thin oxide layers and reduce lifetimes further.[8] The oxide reliability thus remains one of the other major issues in CMOS scaling.[9] It is therefore clear that to meet next-generation device requirements, the solution is represented by using thicker dielectric layers of materials having permittivities higher than that of SiO_2.[7,10,11]

For completely different applications, high-k gate dielectrics are needed in unconventional electronic devices based on organic FETs. As we will describe in detail in the following sections, this research field is also known as "organic" or "printed" electronics. Research and development on organic transistors began in the 1980s with the goal of fabricating electronic circuits by printing all FET materials components instead of defining them using photolithography. If successful, this technology would allow inexpensive, low-temperature, and large area device processing as well as enable new device functions. Thus, simple electronic devices such as radiofrequency identification (RFID) tags and sensors could be fabricated on plastic foils and integrated with commercial item packages in the supply chain.[12−14] Other important printed electronic products include backplane circuitries, which can be used for the fabrication of flexible/bendable displays for e-paper and flexible computers. There are two key interconnected challenges in this area. The first is represented by the limited performance, particularly carrier mobility, of FETs based on printable organic semiconductors. As compared to single-crystal inorganic semiconductors, charge transport efficiency in these materials is reduced by the absence/limited formation of delocalized electronic bands, even in molecular crystals. Because of this limitation, the second key challenge is related to the unacceptably large power (operating voltages) needed to achieve useful FET currents when conventional gate insulators are utilized. A solution to reduce the operating voltages is to enhance gate dielectric capacitance (the drain current scales with the gate capacitance) and, therefore, to employ high-k materials. Finally, note that the dielectric material also indirectly affects FET charge transport characteristics in the semiconductor because of the different charge trapping capacities for holes and electrons.[15,16]

This Review Article focuses on the importance, development, and implementation of high-k gate dielectrics for modern organic electronics applications. We begin by describing the basics and the theory of dielectrics followed by the operating principles of OFET devices to understand the motivations behind improving the dielectric layer permittivity. Next, an overview of the state-of-the-art FET performance achieved using several classes of organic, inorganic,

and hybrid high-k dielectrics will be presented. Several strategies that are utilized to enhance not only k but also the gate capacitance by reducing the layer thickness will be covered. In this contribution, self-assembled mono- and multilayer nanodielectrics will also be described. Finally, throughout this Review, we will also discuss theoretical models and recent experimental data analyzing the effect of the k on the charge transport properties of the semiconductor.

1.1. Theory of Dielectrics

Insulators or dielectric materials are characterized by the absence of charge transport.[17] Nonetheless, when an electric field is applied, these materials undergo a shift in charge distribution. This field-induced polarization leads to dielectric behavior and hence to capacitance, C. If we imagine two electrodes separated by a distance d in a vacuum, the application of a voltage between them creates an electric field that is described by $E = V/d$. The charge created per unit area is proportional to this electric field, as given by eq 1.

$$Q = \varepsilon_0 E = \varepsilon_0 V/d \tag{1}$$

The proportionality constant between the applied voltage and the charge is called the capacitance C, and it is described by eq 2.

$$C = Q/V = \varepsilon_0/d \tag{2}$$

When a dielectric material in inserted between the electrodes, the capacitance is increased (by a factor of k, relative dielectric constant) due to the polarizability of the dielectric. In this case, the capacitance is described by eq 3.

$$C = \varepsilon_0(k/d) \tag{3}$$

Electronic conduction in insulating materials has been a subject of considerable interest in the quest to understand charge transport in the thin film layers of organic electronic devices. In typical dielectric materials, the electronic states near the Fermi level are usually localized states, and the electron wave functions decay exponentially over a distance known as the localization length.[18] In constrast, metals have a high, generally uniform density of states, whereas semiconductors have well-separated conduction and valence bands (separated by a band gap). In a thin film transistor, there exist different junctions, metal−insulator, insulator−semiconductor, and semiconductor−metal, that must be fully understood to optimize the device performance characteristics. In this Review, we will focus exclusively on conductor−dielectric interfaces. As we shall see, several theoretical models have been developed to explain conduction through these junctions.

1.1.1. Coherent Tunneling or Quantum Tunneling

These terms relate to the probability of the electron to cross a dielectric barrier of height, ϕ, and thickness, d. This transport occurs when the dielectric layer thickness is not much greater than the localization length, and then the presence of localized states does not significantly alter the conduction process. As a consequence of this situation, the rate of coherent tunneling decreases exponentially with the dielectric thickness, and the current density through the channel is given by the Simmons relation[19] of eq 4.

$$J_{DT} = \frac{q^2 V}{h^2 d}(2m\phi)^{1/2} \exp\left[\frac{-4\pi d}{h}(2m\phi)^{1/2}\right] \tag{4}$$

Here, J is the current density through the channel (A/cm^2), q is the electron charge, h is Planck's constant, and m is the electron mass. This equation, which contains only a linear term for a rectangular tunneling barrier, accounts for the exponential dependence of the current density on the thickness (d) and the barrier height (ϕ) and describes "through space" tunneling.

In some cases, electron−phonon interactions or interactions of the electron with the orbitals and the electronic structure of the molecule must be taken into account. Theoretical models that account for these interactions have been developed independently by different groups.[20] In this case, "through bond" tunneling becomes more efficient than "through space" tunneling.

Under high electric fields (exceeding the barrier height), the tunneling rate increases, and Fowler−Nordheim tunneling or "field emission" is induced. In this case, it is necessary to modify the rectangular tunneling barrier of the Simmons equation to a triangular shape, as in eq 5, which describes the density current at high E.

$$J_{FN} = \frac{q^3 E^2}{8\pi h \phi_{FN}} \exp\left[\frac{-4\sqrt{2m^*}}{3qhE}(q\phi_{FN})^{3/2}\right] \tag{5}$$

Here, ϕ_{FN} is the tunneling barrier height, E is the electric field (V/cm), and m^* is the effective electron mass. This tunneling is basically independent of temperature and also decreases exponentially with distance,[19,21] as in the Simmons equation. Both equations presented in this section only apply for very thin dielectric layers;[22] when the thickness increases sufficiently, other transport mechanisms must be considered. In fact, these are the mechanisms usually found for transport through self-assembled monolayers.[23]

1.1.2. Incoherent, Diffusive Tunneling

In the case of a thick barrier and a high density of localized states, it is necessary to consider the probability of the electron tunneling resonantly between two or more consecutive sites that are characterized by potential wells.[24] The process in this case may be viewed as a series of discrete steps (see Figure 1).[25] The mechanism can be considered to be independent of temperature and should be in principle the predominant one in the limit of very thick barriers at extremely low temperatures.[18]

1.1.3. Hopping Mechanisms

These mechanisms are usually thermally activated electron transfers and are dominant at low fields and moderate temperatures. They follow the classical Arrhenius model (eq 6):

$$\sigma = \sigma_0 \exp\left(\frac{-E_a}{k_B T}\right) \tag{6}$$

Here, σ is the conductivity ($\sigma = J/E$), E_a is the activation energy, and k_B is the Boltzmann constant. This mechanism is similar to the diffusive tunneling process in that the electron travels between one or more sites. The major difference is that the hopping involves nuclear motion.[26,27]

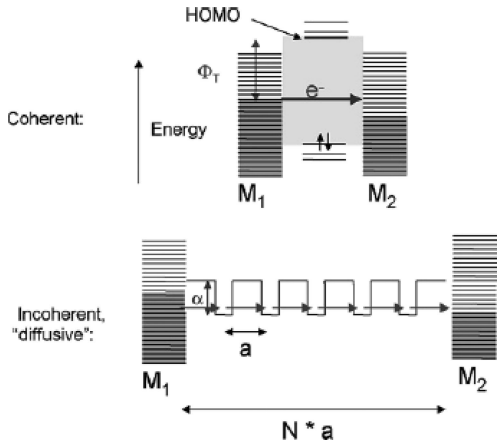


Figure 1. Schematic energy level diagrams for coherent and diffusive tunneling between two metals M_1 and M_2. Φ_T is the barrier for coherent tunneling, and α is the potential well depth of N sites spaced apart by a distance a. Reproduced with permission from ref 25. Copyright 2004 American Chemical Society.

The electron transfer occurs over the barrier, following the dependence on driving force predicted by Marcus theory.[28] Because this process involves a series of hopping sites, this thermally activated mechanism does not exhibit the exponential distance dependence found in coherent tunneling, but it varies in proportion to d^{-1}. That means that for larger d, the distance is too great for coherent tunneling, and the electron propagates more efficiently by hopping between "hopping" sites.

1.1.4. Poole−Frenkel Effect

This approach was developed to account for the effects of "traps" in hopping electron transport. The Poole−Frenkel effect is attributed to the lowering of trapping Coulombic barriers within the molecule by the applied electric field, and it explains the electric current in semiconductors.[19a,21,29] The trapped electrons contribute to the current density according to the Poole−Frenkel equation (eq 7) at high temperatures and intermediate fields.[30]

$$J_{PF} = \sigma_0 E \exp\left[\frac{-q(\phi_B - \sqrt{qE/\pi k})}{k_B T}\right] \quad (7)$$

In this equation, W is the electric field ($E = V/d$), σ_0 is the low field conductivity, ϕ_B is the Frenkel−Poole barrier height, k is the dielectric permittivity, and k_B is the Boltzmann constant.

1.1.5. Schottky Emission

This theory explains the electron transfer mechanism at interfaces.[31] A Schottky barrier arises from partial charge transfer from one layer to the other at an interface. As a result, a depletion layer or electrostatic barrier is generated. The Schottky emission or thermoionic emission is described by eq 8, and it considers that an electron can be injected through the interface once it has sufficient thermal energy to surmount the potential height.[32]

$$J_S = A^* T^2 \exp\left[\frac{-q(\phi_S - n\sqrt{qE/4\pi\varepsilon})}{k_B T}\right] \quad (8)$$

In eq 8, A^* is the modified Richardson's constant ($A^* = 120$ A/cm^2·K^2), n is the diode ideality factor, E is the electric field, ϕ_S is the Schottky barrier height, ε is the dielectric permittivity, and k_B is the Boltzmann constant.

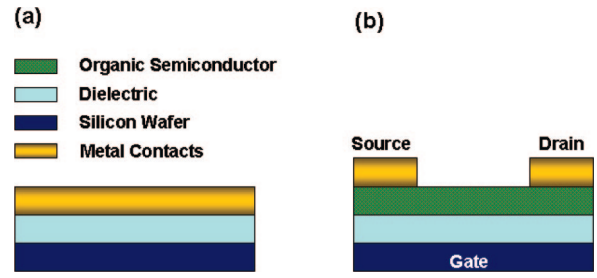


Figure 2. Typical structures of (a) organic-based capacitors and (b) organic field-effect transistors.

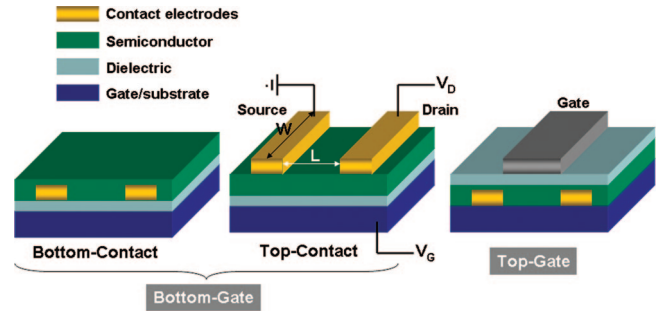


Figure 3. Different structures of organic field-effect transistors. L, channel length; W, channel width.

1.2. General Applications

Dielectrics are widely used in numerous applications. The most fundamental of these is their use as an insulating layer against electrical conduction. To be an insulator, a material must have a large band gap. In that way, there are no states available into which the electrons from the valence band can be excited. Nonetheless, there is always some voltage (the breakdown voltage) that will impart sufficient energy to the electrons to be excited into this band. Once this voltage is surpassed, the dielectric will lose its insulating properties.

The other two major applications of dielectrics are in capacitors[33] and transistors, both of which are essential components of electronic circuits. The structures of both of these electronic devices are shown in Figure 2. A capacitor is a passive electrical component consisting of a dielectric sandwiched between two conductors. The application of a voltage across this material will, at electric fields lower than the breakdown field of the dielectric (typically several MV/cm),[34,35] induce a charge separation across the insulating layer forming the capacitor.[21,34] An ideal capacitor is characterized by a single constant parameter, the capacitance C. Higher C values indicate that more charge may be stored for a given voltage. Nonetheless, real capacitors are not complete insulators and allow a small amount of current flowing through, called leakage current.

The OFET structure (Figure 2b) is similar to the capacitor structure but having an additional semiconductor layer (organic in the case of OFETs) in contact with the gate dielectric.

2. Field-Effect Transistors and Organic Field-Effect Transistors

Figure 3 shows the common device configurations used in field-effect transistors (FETs). These configurations can be either bottom-gate or top-gate. In the first configuration

(bottom-gate), two different structures can be used, bottom-contact or top-contact, depending on the position of the source and drain electrodes. In the case of organic field-effect transistors (OFETs), the semiconductor layer is an organic material.

Because there are a large number of excellent reviews that explain the basis of OFET function in detail, in this Review we will only comment on these aspects briefly.[36] In principle, the characteristic that best defines an OFET is the presence of an electric field that controls and modulates the conductivity of the channel between the source and drain. In the devices shown in Figure 3, this electric field is created by the voltage applied between the source and gate, the gate voltage (V_G), but is also dependent on the insulator/dielectric layer. Indeed, a positive/negative gate voltage will induce negative/positive charges at the insulator/semiconductor interface, and the number of these accumulated charges depends on V_G and on the capacitance C of the insulator. When no voltage is applied between the source and gate ($V_G = 0$), the device is "off". On increasing both V_G and V_D (voltage between source and drain), a linear current regime is initially observed at low drain voltages ($V_D < V_G$) (eq 9) followed by a saturation regime at higher V_D values (eq 10).

$$(I_{SD})_{lin} = (W/L)C(V_G - V_T - V_D/2)V_D \quad (9)$$

$$(I_{SD})_{sat} = (W/2L)C(V_G - V_T)^2 \quad (10)$$

In these equations, $(I_{SD})_{lin}$ is the drain current in the linear regime, $(I_{SD})_{sat}$ is the drain current in the saturation regime, μ is the field-effect carrier mobility of the semiconductor, W is the channel width, L is the channel length, C is the capacitance per unit area of the insulator layer, V_T is the threshold voltage, V_D is the drain voltage, and V_G is the gate voltage.

The above equations indicate that the current between the source and drain can be increased by increasing either V_G or V_D. Nonetheless, these two parameters can be increased to only a certain extent. As is also evident in eqs 9 and 10, another viable approach to minimizing V_G and/or increasing the electrical current is adjusting the capacitance of the gate dielectric, C, as described by eq 3. This relationship makes it clear that by either increasing k or decreasing d, the device current is enhanced. Note also that a small d is required in devices using short channel lengths. Typically, $d/L \leq 0.1$ is necessary to ensure that the field created by V_G, and not the lateral field V_D, determines the charge distribution within the channel.[37] Several groups have adopted the approach of reducing dielectric thickness to realize low-voltage operation OFETs. For example, Vuillaume et al. employed an organic monolayer of carboxyl-terminated alkyltrichlorosilanes (thickness range 1.9−2.6 nm) with linear end groups for the gate dielectric to achieve working voltages below 2 V.[38] Halik et al. demonstrated low-voltage organic transistors using self-assembled monolayers (SAMs) of (18-phenoxyoctadecyl)-trichlorosilane, thereby enhancing the mobility of pentacene devices to $\sim$1 cm^2 V^{-1} s^{-1} due to favorable interactions at the semiconductor−dielectric interface.[39] Finally, Marks et al. studied self-assembled multilayers (SAMTs) grown from solution to achieve very low leakage currents and low operating voltages.[40]

Other figures-of-merit that must also be optimized in OFET devices are the threshold voltage, I_{ON}/I_{OFF} ratio, and subthreshold slope ($S = dV_G/d(\log I_D)$), related to how efficiently the gate field modulates the "off" to "on" current and how abruptly the device turns "on". These parameters depend not only on the nature of the organic semiconductor but also on the chemical structure and dielectric properties of the insulator used, and on the capacitance resulting from interface traps, C_{IT}, as shown in eq 11 for S.[41]

$$S = \frac{k_B T}{e} \ln(10)(1 + C_{IT}/C) \quad (11)$$

2.1. Dielectric Effects on the Figures-of-Merit of OFET Devices

There are specific requirements for gate dielectrics to be used in field-effect transistors. Apart from a high capacitance, as shown in Section 2, high dielectric breakdown strength,[42] high levels of purity, high on/off ratios, low hysteresis, materials processability, and device stability are essential.[43]

To understand the role of the gate dielectric on FET device figures-of-merit, it is important to take into account that most relevant processes taking place in these devices (charge accumulation and transport) occur in close proximity to the interface between the gate dielectric and the semiconductor layer. This implies that an optimum dielectric−semiconductor interface is fundamental for efficient device function. For example, threshold voltages normally depend strongly on the semiconductor and dielectric used because impurities and charge trapping sites tend to increase this value. It is also quite clear from eqs 9 and 10 that V_T can be easy modulated by increasing the capacitance of the dielectric, which creates a higher density of charges in the interface at lower voltages. Several authors have also suggested that by controlling the density of semiconductor−dielectric interface states, it should be possible to modulate threshold voltages in organic transistors.[44]

The nature of the insulator interface has also been widely shown to have a great impact on the semiconductor mobility,[45] as was first demonstrated by the deposition of pentacene on SiO_2 under different growth conditions.[46,47] The polarity of the dielectric interface can also influence the quality of the semiconductor layer, affecting local morphology, the density of states (DOS) in the organic semiconductor layer, and, consequently, the field-effect mobility. The latter effect was extensively analyzed by Veres et al.[48] on amorphous polymer-based OFETs. In their study, they investigated a number of gate insulators having varying polarity using polytriarylamines (PTAA) and poly(9,9-dioctylfluore-*co*-bithiophene) as the semiconductor materials, and they found that device performance was significantly increased when the insulator permittivity was below 2.5 (see Figure 4). The authors ascribed this fact to an increase of carrier localization by electronic polarization in the high-k dielectrics. To explain this phenomenon, Veres et al. proposed the graphical illustration in Figure 4b, where the DOS is shown as a Gaussian distribution of localized states. As illustrated in Figure 4b, as the dielectric−semiconductor interface becomes more polar, the DOS broadening becomes more severe, leading to more tail states. The authors pointed out that this effect can be only applied to organic materials where the formation of electronic bands is very limited, because random dipoles are unlikely to significantly affect the extended states of a wide band. The theoretical approach to this qualitative explanation has been recently developed by Richards et al.[49] In their work, the authors calculated the broadening of the DOS due to dipolar disorder using an analytical model as a

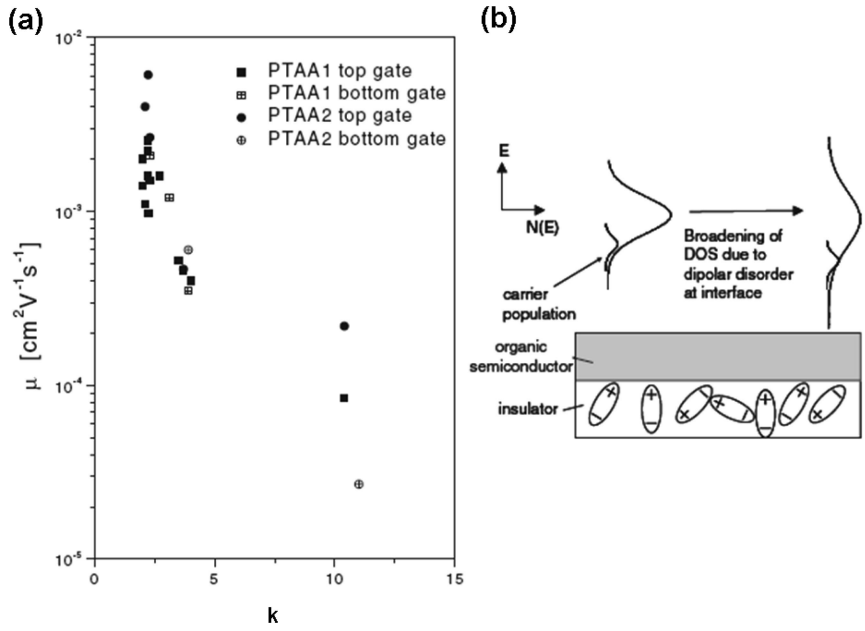


Figure 4. (a) FET mobility of PTTA-based OFETs as a function of gate insulator permittivity (k) for top- and bottom-gate structures. (b) Suggested mechanism for the enhancement of carrier localization due to polar insulator interfaces. Reproduced with permission from ref 48. Copyright 2003 Wiley−VCH Verlag GmbH & Co. KGaA.

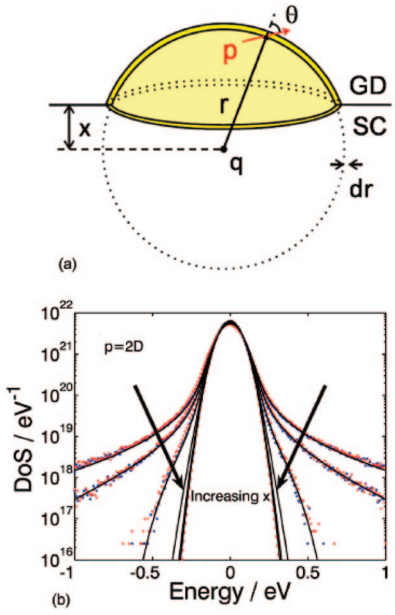


Figure 5. (a) Schematic illustrating the interaction of the charge q in the semiconductor (SC) with a dipole moment p in the gate dielectric (GD). The charge in the semiconductor is located at a distance x away from the interface. (b) Calculated DOS broadening due to static dipolar disorder in the dielectric with increasing distance into the semiconductor. Each line corresponds to a step of 1 Å into the semiconductor from $x = 0$ to $x = 5$ Å. The dots are a result of numerical simulation including either just the nearest dipole ($n = 1$, blue squares) or the nearest 10 dipoles ($n = 10$, red circles). Reprinted with permission from ref 49. Copyright 2008 American Institute of Physics.

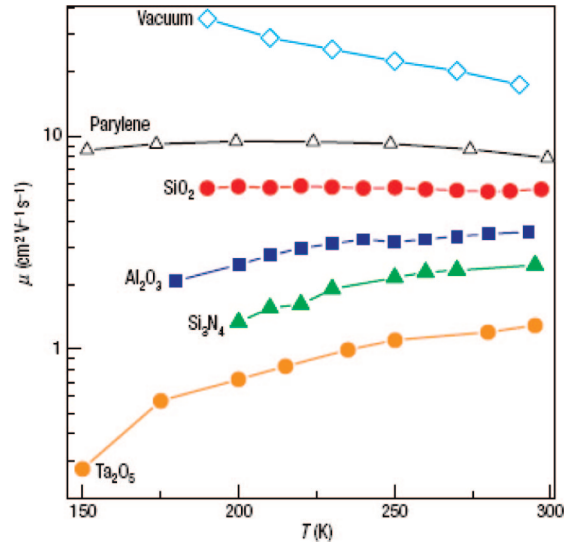


Figure 6. Temperature dependence of the carrier mobility for single-crystal rubrene FETs with six different gate dielectrics. Reprinted with permission from ref 51a. Copyright 2006 Macmillan Publishers Ltd.

function of the distance from the interface, and they demonstrate that the interaction of the charge with the dielectric environment is dominated by the nearest dipoles in the dielectric layer (Figure 5a). The authors also model the dependence of the PTAA field-effect mobility on the dipolar disorder broadening using a Gaussian disorder model[50] and obtain a good quantitative agreement with the experimental data, which is surprising because the model does not include fitting parameters. These results fully support the previous work by Veres et al.[48] and may also explain the enhancement of mobility by SAM surface treatment because this thin layer could substantially reduce the interaction of the charges with the dipoles in the dielectric.

A different explanation for the dependence of mobility on k has been proposed by Hulea et al.[51] In their work, the temperature dependence of the mobility for single-crystal rubrene-based FETs is shown for six different gate insulators ranging in k from 1 to 25. As previously reported by Veres et al.,[48] the mobility decreases with the dielectric constant of the gate insulator (see Figure 6), and they reported a crossover from "metallic-like" to "insulating-like" behavior of the mobility dependence on temperature as k increases. In this case, the μ dependence on k is attributed to charge localization and the formation of Fröhlich polarons at the

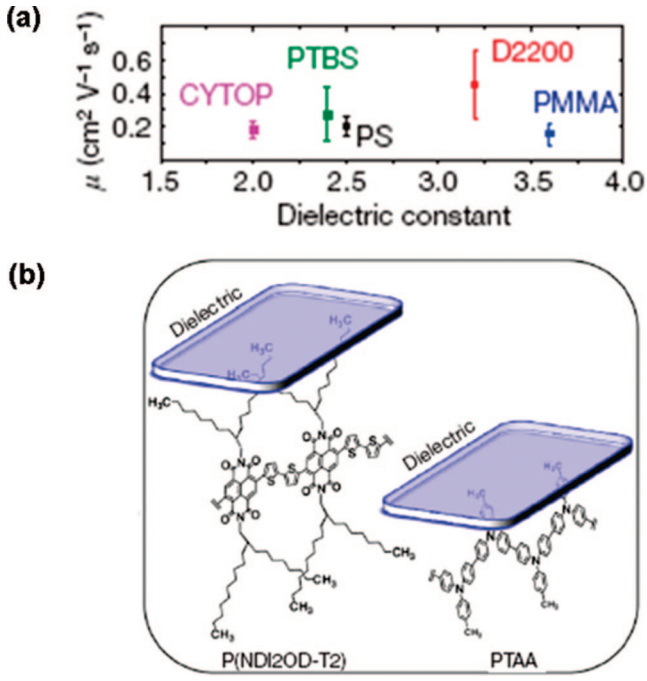


Figure 7. (a) Plot of the average electron mobility of P(NDI2OD-T2)-based OFETs versus the dielectric constant of the gate dielectric. (b) Schematics of P(NDI2OD-T2) and PTAA polymers below the gate dielectric surface. Reprinted with permission from ref 52. Copyright 2009 Macmillan Publishers Ltd.

semiconductor−dielectric interface and is supported by theoretical calculations. This effect was also considered by Richards et al.[49] in their theoretical approach to explain the mobility dependence of PTTA-based OFETs, and they argue that the polaron effect makes only a small contribution to the lowering of the mobility with increasing gate voltage in the case of an amorphous polymer.

In contrast to the above results, Yan et al.[52] found little sensitivity of the mobility of poly{[*N*,*N*′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)2,6-diyl]-*alt*-5,5′-(2,2′-bithiophene)} (P(NDI2OD-T2)-based OFETs to different gate dielectrics ranging in k from 2.1 to 3.6 (Figure 7). The authors ascribe this fact to the different attachment of PTAA and P(NDI2OD-T2) polymers to the dielectric surface (see Figure 7b). The significant decoupling of the latter polymer from the dipoles within the dielectrics, due to the existence of long branched substituents, is the reason that the authors proposed to explain the substantial k-insensitive mobility behavior.

Finally, one of the most characteristic parameters of the dielectric layer is the gate leakage that determines the current when the device is in the "off" state (I_{OFF}). The leakage current then determines the ratio I_{ON}/I_{OFF} which must be as high as possible for proper switching of the device. Leakage usually increases power consumption, which is undesirable in practical devices. Great efforts are being taken worldwide to minimize leakage currents, and these include the use of strained silicon and high-k dielectrics. Furthermore, leakage control to continue Moore's law[53] reduction will not only require new materials but also device optimization. Leakage increases exponentially as the thickness of the insulation layer decreases; however, a thicker insulator layer will decrease the capacitance of the dielectric. This consideration indicates that the thickness of the insulator must be carefully controlled to obtain the maximum performance. In this regard, the Northwestern group has made a major effort to modulate the thickness of self-assembled nanodielectrics (SANDs), which with the sequential deposition of successive monolayers (type I, type II, and type III) yields high-performance dielectrics having the desired characteristics (see Figure 25).[36g]

2.2. Interface Trapping Effects

As was already discussed above, structural ordering at the semiconductor−dielectric interface is extremely important to FET function because poor molecular order causes severe degradation of the transport properties,[54] often affecting the structural ordering of the overlying semiconductor film as well.[55] In this sense, several experimental studies have shown that the difference in the charge transport observed between bulk organic semiconductors and that in the channel near the gate−insulator interface in OFETs is associated with the effects of disorder and interfacial traps.[56,57] In the organic electronics field, to analyze the effects of interfacial order, several groups have used pentacene transistors, because this organic semiconductor is one of the most studied and has a mobility comparable to that of amorphous silicon.[58,59] Indeed, Wang et al. demonstrated that the threshold voltage in pentacene-based devices can be tuned via chemical modification of the gate dielectric layer.[44] They found that oxygen plasma treatment of the organic polymer gate dielectric, parylene, introduces traps at the semiconductor−dielectric interface that strongly affect OFET performance. The O_2 treatment breaks bonds at the parylene surface, introducing semiconductor−dielectric interface states. These states create mobile charges, Q_{mobile}, which increase parasitic bulk conductivity in the device but also introduce fixed charges, Q_{fixed}, which are responsible for the V_T shift. The presence of these traps also modifies the capacitance of the dielectric layer and not only by O_2 plasma erosion of the thickness. In fact, the traps can be modeled as capacitances with time constants related to the trapping and release of the carriers.[60] Wang et al. calculated the total capacitance as a combination of three capacitances as shown in eq 12. For the pentacene (semiconductor), the depletion capacitance is C_S, the capacitance of traps at the dielectric−semiconductor interface is C_{it}, and the dielectric capacitance is C.

$$C_{total} = \left(\frac{1}{C_S} + \frac{1}{C + C_{it}}\right)^{-1} \quad (12)$$

The mobility can then be calculated according to eq 13:

$$-I_D = \frac{W}{L}\mu V_D[(V_G - V_T)C - Q_{fixed} + Q_{mobile}] \quad (13)$$

Daraktchiev et al. have fabricated a model organic field-effect transistor that is basically composed of a single layer of a pentacene crystal in interaction with an oxide surface,[47] and they suggest that an equilibrium between free and trapped carriers at the oxide interface determines the OFET performance characteristics. This ultrathin layer of pentacene exhibits continuous coverage by adjacent pentacene islands and minimal interisland boundary density, indicating that it interacts strongly with the oxide surface. In this case, they suggested that the oxide is not just a homogeneous passive dielectric but an active surface in the sense that electroactive surface defects and radicals can act as either electron acceptors or hole traps.[47,48] This picture is also supported

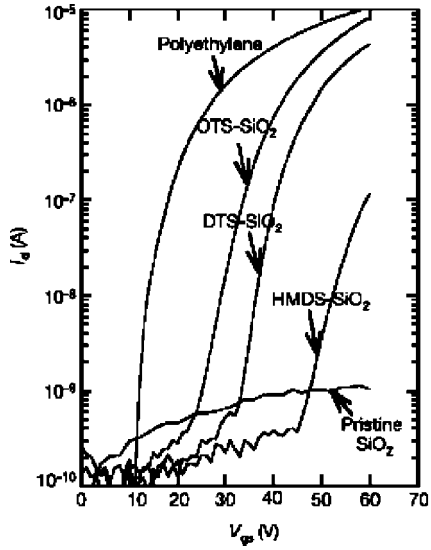


Figure 8. Transfer characteristics of poly(9,9-dioctylfluorene-*alt*-benzothiadiazole)-based FETs with various siloxane self-assembled monolayers on SiO_2 as dielectric or with polyethylene as buffer dielectric. DTS: decyltrichlorosilane. Reprinted with permission from ref 15. Copyright 2005 Macmillan Publishers Ltd.

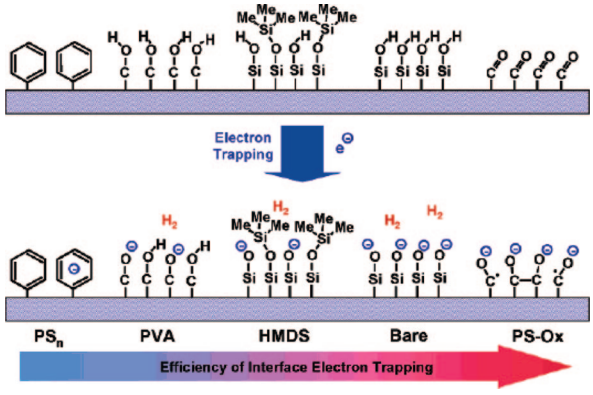


Figure 9. Schematic diagram of functional group electron trapping efficiency on various bilayer dielectric layers. Reprinted with permission from ref 61. Copyright 2006 American Chemical Society.

by the results of Friend et al. who demonstrated that the reason why n-type behavior is typically difficult to achieve is due to electron trapping at the semiconductor−interface by hydroxyl groups in the case of commonly used SiO_2 dielectrics.[15] In this work, Friend et al. showed that using SAM-modified SiO_2 substrates diminishes the density of surface trapping SiOH groups, thereby increasing mobility (see Figure 8) and even enabling ambipolar operation.

A subsequent study by Yoon et al.[61] supported the previous findings by evaluating the OFET response characteristics of six organic semiconductors grown on four different SiO_2−polymer bilayer dielectric structures and comparing the results to HMDS-functionalized and pristine SiO_2 dielectrics (see Figure 9). For each gate dielectric examined, they could estimate a different efficiency of interface electron transport as shown in Figure 9, which in turn enabled differing modulation of the device performance. Significant variations in modulation of the field-effect mobility with the semiconductor type (air-sensitive p-type, air-stable p-type, and n-type semiconductors) were also reported. The authors found that polystyrene coatings on SiO_2 greatly enhance the mobilities of overlying air-sensitive n-type semiconductors, achieving a mobility as high as ~2 $cm^2\ V^{-1}\ s^{-1}$ for α,ω-diperfluorohexylcarbonylquaterthiophene (versus 0.4 $cm^2\ V^{-1}\ s^{-1}$ for HMDS-treated SiO_2 substrates). Yoon et al. ascribed this mobility sensitivity to differences in electron trapping at the semiconductor−dielectric interface. In contrast, the improvement was nominal in the case of air-stable n-type and p-type semiconductors.

A recent study by Hill et al. demonstrated that simply changing the SiO_2 dielectric cleaning method (solvent cleaning vs oxygen plasma treatment) yields different device performance parameters, with superior results measured for oxygen plasma treatment.[62] This improvement is attributed to the reduction in organic contamination at the semiconductor/dielectric interface after the plasma cleaning, and a corresponding reduction in both hole and electron interfacial trapping states.

As was already noted in the previous section, several groups have also reported a substantial decrease in the mobility of different semiconductors as the gate insulator dielectric constant is increased,[48,51b] suggesting an effect due to strong interactions of the charge carriers with the gate dielectric. Houili et al.[63] suggested that this dielectric constant dependence may occur through modification of the trap state energetics and distributions by the presence of a polarizable interface. This result suggests that the mobilities of devices fabricated with a polymer gate insulator should be larger than those using high-permittivity oxide gate dielectrics. Photo and electrical instability have also been attributed in some cases to the electron trapping ability of some dielectric films.[64] Furthermore, the appearance of gate voltage-dependent mobility, together with variations in threshold voltages,[65] has been also usually attributed to dielectric interface effects.[66]

The presence of grain boundaries in thin semiconducting films cannot be neglected, because they can have a significant influence on the measured mobility[67] as well as on the subthreshold slope, and it is related to grain size. Nevertheless, the exact effects of grain size on the device performance remain unclear,[36g,48,68,69] despite the fact that correlations between pentacene film grain size/crystallinity and OFET performance have been studied in great detail.[12c,70,71] However, what is unequivocal from all of these results is that the pentacene grain growth can be modulated by using different dielectrics and dielectric surface treatments.

3. High-k Dielectric Materials for OFETs

3.1. Inorganic Dielectrics

The most common gate dielectrics used in both academia and industry are Si substrates having SiO_2 layers (typically 200−400 nm thick).[72] The utilization of this dielectric is very convenient due to the ready availability of the thermally grown dioxide. In fact, silicon can be reacted with oxygen or nitrogen in a controlled manner to form superb insulating layers with excellent mechanical, electrical, and dielectric properties. Recently, it has been shown that the semiconductor−dielectric interface in these devices contains a large density of electron-trapping sites due the existence of surface hydroxyl groups, which are present in the form of silanols.[15] Neutralization of these sites has been partially solved using surface treatments in which a monolayer is self-assembled on the SiO_2 surface. High advancing aqueous contact angles (>90°) have been measured using hexamethyldisilazane (HMDS),[73] alkanetrichlorosilanes,[74] and alkanephosphonic

acids[39,75] -based self-assembled monolayers (SAMs), among others. A concurrent decrease in the density of interfacial trap sites is observed, leading to improved FET performance for some n-type semiconductors.[15] These and other SAMs will be briefly summarized in a subsequent section, but first we will focus on the use of high-k inorganic dielectrics.

The interest in new dielectric materials has arisen primarily from the necessity for inexpensive device fabrication processes and the reduction of the operating voltages required for new flexible/printed electronics technologies. In fact, one of the major challenges in the development of OFETs has been the rather high voltages needed for their operation when using SiO_2 gate dielectrics ($k \approx 4$), making these devices impractical for low-priced applications. The key to low-voltage application resides in the reduction of the threshold voltage and the inverse subthreshold slope. Both parameters are basically controlled by the gate insulator. It is thus mandatory to search for thin, high-k gate dielectrics to achieve the requirements needed for new technologies. One of these requirements is reduction of the device size that can be also achieved using high-capacitance gate insulators. In this sense, SiO_2 has reached its scaling limit,[76] directing the study of many groups in the search for alternative metal oxides (HfO_2, Ta_2O_5, Al_2O_3, Y_2O_3, CeO_2, TiO_2, etc.) as alternative insulator layers.

Although the idea of using high-k dielectrics for improving the performance of organic electronic devices is implicit in the fundamental equations describing FET performance, relatively little work had been done until recently with these kinds of insulators in organic FETs. However, high permittivity dielectrics have been extensively used in inorganic FETs.[77] Dimitrakopoulos et al.[78] were the first to use high-k oxides as dielectrics in OFETs. They used different thicknesses of SiO_2, sputtered amorphous barium zirconate titanate (BZT, k (bulk) = 17.3), barium strontium titanate (BST, k (bulk) = 16), and Si_3N_4 (k (bulk) = 6.2) as gate dielectrics to fabricate pentacene OFETs. In this work,[78b] the authors determined that the pentacene field-effect mobility could be increased by using high-k dielectrics (see Figure 10a), because a higher concentration of accumulated carriers in the channel region can be achieved at lower voltages. Furthermore, due to the possibility of a low temperature fabrication process for BZT gate insulators, they successfully fabricated pentacene-based OFETs on high-transparency plastic substrates (polycarbonate), achieving mobilities ranging from 0.2 to 0.38 $cm^2\ V^{-1}\ s^{-1}$ at operating voltages below 5 V (Figure 10b). Since then, many groups have pursued the development of metal oxide dielectrics to be used in organic electronics (see Table 1).

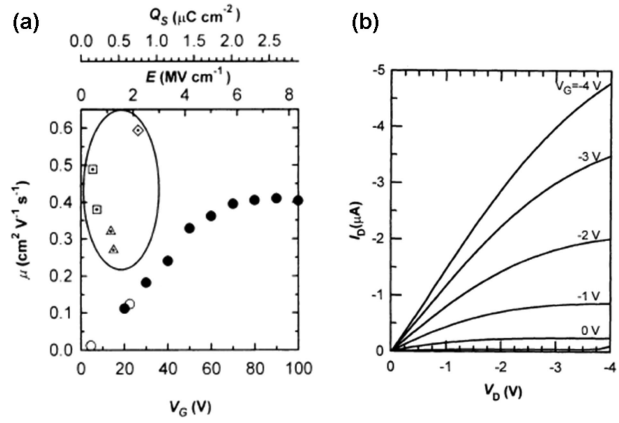


Figure 10. (a) Dependence of field-effect mobility of various pentacene-based OFETs on V_G, gate field E, and charge per unit area on the semiconductor Q_S. The "●" symbols refer to all three x axes and correspond to devices with 0.12 μm thick SiO_2. The "○" symbol refers only to the E and Q_s axes (0.5 μm thick SiO_2). Data points in the ellipsoid refer to the E axis only. Triangles are BZT-based OFETs, squares are BST-based OFETs, and diamonds are Si_3N_4-based OFETs. (b) Output plot of a pentacene-based OFET on a polycarbonate substrate. Reprinted with permission from ref 78b. Copyright 1999 AAAS.

3.1.1. Aluminum Oxide

The use of Al_2O_3 as an OFET gate dielectric ($k = 8$) was first reported by Im's group in 2002 using radiofrequency (rf) magnetron sputtering at various deposition temperatures (RT, 200, and 300 °C) to fabricate the oxide layer.[79] They reported that Al_2O_3 offers higher capacitance than thermally grown SiO_2, exhibiting optimum performance (leakage current and surface roughness) when deposited at room temperature. One year later, the same group fabricated pentacene-based OFETs using room-temperature rf-magnetron sputtered Al_2O_3 dielectric films on tin-doped indium oxide (ITO).[80] The optimized devices showed good electrical performance, with a hole mobility of 0.14 $cm^2\ V^{-1}\ s^{-1}$, a subthreshold slope of 0.88 V dec^{-1}, and an I_{ON}/I_{OFF} ratio greater than 10^6. These were promising results that pointed out the potential of this metal oxide as a gate dielectric material in flexible organic electronics because good quality films could be obtained using room-temperature processes. Indeed, Majewski's group[81] later demonstrated the possibility of fabricating flexible OFET devices by depositing anodized Al_2O_3 dielectrics on flexible Al/Mylar substrates. For films with an anodization voltage of 100 V, they measured a capacitance of ~60 nF cm^{-2} and leakage current lower than 10^{-9} A cm^{-2}. Higher capacitances (600−700 nF cm^{-2}) were measured for a 6.5 nm thick dielectric film. In this article, Majewski demonstrated that the thickness of the resulting films can be controlled very precisely via the anodization voltage and that pinholes heal themselves during the anodization process, resulting in high-quality dielectric oxides. In subsequent work, they modified the interface by the self-assembly of an octadecyltrichlorosilane (OTS) monolayer or by the deposition of a thin poly(α-methylstyrene) layer, finding characteristics similar to those reported for thermally grown silicon oxide.[82] To explain the mobility enhancement by surface modification, temperature-dependent mobility measurements were carried out, suggesting that the deposition of the additional organic layer induces a change in the morphology of the semiconductor.[82] In the same area of flexible devices, the compatibility of anodized Al_2O_3 with a variety of polymeric substrates has been investigated for the fabrication of polymeric and molecular-based OFETs.[83] More recently, also using anodized Al_2O_3, a low-temperature process for an active-matrix organic thin-film transistor polymer dispersed liquid crystal display was reported.[84] The thickness of the gate dielectric was 60 nm with a dielectric constant of 9. The field-effect mobility for pentacene-based devices was reported to be 0.2 $cm^2\ V^{-1}\ s^{-1}$.

In 2004, Im's group reported on the electrical properties of pentacene-based OFETs using aluminum oxide films deposited by rf magnetron sputtering on ITO glass.[85] They deposited the semiconductor at different temperatures and found that the thickness of the pentacene layer increases with increasing substrate temperature, accompanied by a phase

Table 1. Summary of the Dielectric Properties (Thickness, D; Capacitance, C_i; Dielectric Constant, k; and Breakdown Field, E_B) and OFET Characterization (Mobility, μ; Current On/Off Ratio, I_{ON}/I_{OFF}) for Various Inorganic Gate Dielectrics

ref	dielectric	method[a]	D (nm)	C_i (nF cm^{-2})	k	E_B (MV/cm)	semiconductor	μ (cm^2 V^{-1} s^{-1})	I_{ON}/I_{OFF}	year
78	BZT	sputt.			17.3		pentacene	0.32	10^{+5}	1999
	BST	sputt.			16		pentacene	0.4−0.5		
	Si_3N_4	sputt.			6.2		pentacene	0.6		
91	Ta_2O_5	anodiz.	∼50		23	4−5	DH5T	0.03		2000
							FPcCu	0.02		
92	Ta_2O_5	e-beam	100		21	>1	P3HT	0.02		2002
80	Al_2O_3	sputt.	270		7	3	pentacene	0.14	10^{+6}	2003
93	Ta_2O_5	anodiz.	86−188	109−248	23−27		pentacene	0.36	10^{+4}	2003
94	Ta_2O_5	sputt.		66			PcCu	0.01		2003
95	Ta_2O_5	anodiz.	130				6−6′-dihexyl-[2−2′]bianthracene	0.22	10^{+6}	2003
82	Al_2O_3+PAMs	anodiz.		260			pentacene	0.3		2004
	Al_2O_3+OTS	anodiz.		250			rr-P3HT	5×10^{-3}		
85	Al_2O_3	sputt.	250		7	3	pentacene	0.2	$2 \times 10^{+5}$	2004
97	Ta_2O_5	anodiz.					pentacene	0.51	10^{+5}	2004
115	ZrO_2	e-beam	250				pentacene	0.12	10^{+4}	2004
	ZrO_2+OTMS	e-beam					pentacene	0.66	10^{+5}	
120	Gd_2O_3	IBAD	280		7.4	−0.3	pentacene	0.1	10^{+3}	2004
98	Ta_2O_5+HMDS	anodiz.	150		23		pentacene	0.2	10^{+5}	2005
105	TiO_2	anodiz.		676			pentacene	0.15		2005
	TiO_2+OTS	anodiz.		465			pentacene	0.25		
	TiO_2	anodiz.		2416			PTAA	$<10^{-5}$		
	TiO_2+OTS	anodiz.		460			PTAA	3.5×10^{-5}		
86	Al_2O_3+HMDS	PEALD	150	41			pentacene	0.14	10^{+5}	2007
88	Al_2O_3+HMDS	PEALD	150				pentacene	0.62	10^{+7}	2007
99	Ta_2O_5	e-beam		325			pentacene	0.45		2007
	Ta_2O_5+HMDS	e-beam		245			pentacene	0.51		
100	Ta_2O_5	sputt.	500	35			vanadyl-phthalocyanine	0.05−0.1	10^{+4}	2007
111	HfO_2	sol−gel	20		11		pentacene	0.13	$5 \times 10^{+3}$	2007
	HfO_2	anodiz.					pentacene	2.2×10^{-2}	$>10^{+3}$	
84	Al_2O_3	anodiz.	60		9		pentacene	0.2		2008
45c	TiO_2	sputt.	97	373	41	∼3	P3HT	5×10^{-3}	10^{+2}	2008
	Al_2O_3		93	79	8.4	∼8	P3HT	6×10^{-3}	10^{+2}	
106	TiO_2	sol−gel			27		P3HT	3.73×10^{-3}	10^{+1}	2008
112	$(HfO_2)_{0.75}(SiO_2)_{0.25}$	ALD	6	1400			pentacene	0.11		2008
	$(HfO_2)_{0.25}(SiO_2)_{0.75}$	ALD	6	600			pentacene	0.11		
113	HfO_2/Si_3N_4	sputt.	50 (HfO_2) + 60 (Si_3N_4)		10.4		pentacene	0.21		2008

[a] Dielectric deposition method. Abbreviations: sputt., sputtering; anodiz., anodization; PEALD, plasma-enhanced atomic layer deposition; ALD, atomic layer deposition.

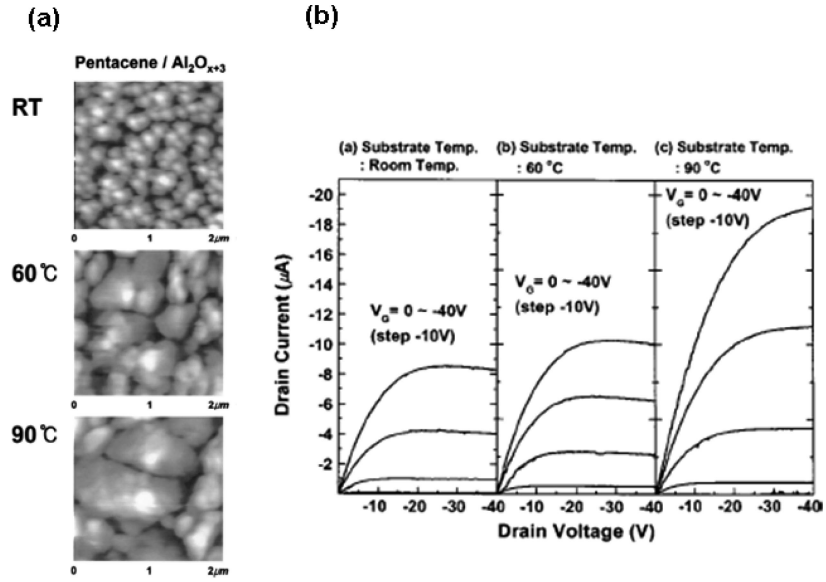


Figure 11. (a) AFM images of pentacene films deposited on Al_2O_{x+3} at 25, 60, and 90 °C. (b) Output characteristics of the pentacene-based OFETs fabricated on Al_2O_{x+3} at 25, 60, and 90 °C. Reprinted with permission from ref 85. Copyright 2004 American Institute of Physics.

transition. Nevertheless, they found no noticeable improvement at higher growth temperatures, only enlarged pentacene grains and increased trap densities in the pentacene channel, increasing leakage current, and shifting V_T (see Figure 11). As a consequence, the mobility was ∼0.20 cm^2 V^{-1} s^{-1} for every temperature, but V_T increased from −1.2 to 5 V on going from 25 to 90 °C.

More recently, another group fabricated pentacene-based OFETs with a 150 nm thick plasma-enhanced atomic-layer-deposited (PEALD) Al_2O_3 film covered by a spin-coated

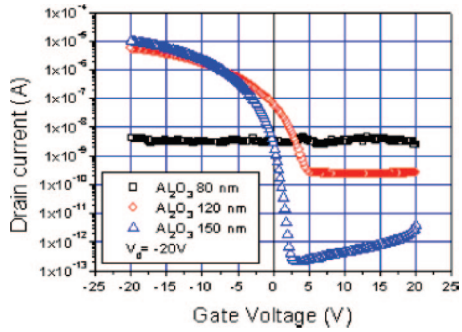


Figure 12. Electrical transfer characteristics of pentacene OFETs with gate dielectric thicknesses of 80, 120, and 150 nm, and $V_D = -20$ V. Reprinted with permission from ref 88. Copyright 2007 The Electrochemical Society.

hexamethyldisilazane-derived thin $-Si(CH_3)_3$ layer as the gate dielectric, obtaining a pentacene mobility of 0.14 $cm^2 V^{-1} s^{-1}$, a threshold voltage of −6.2 V, subthreshold slope of 0.9 V dec^{-1}, and I_{ON}/I_{OFF} of 10^5.[86] In this case, the authors analyzed the hysteresis and stability of V_T, because these represent major challenges for the mass production of practical OFETs. Some hysteresis was observed, and the authors argued that it was due to charge trapping/detrapping near the semiconductor/dielectric interface, as previously suggested by other groups.[87] Nevertheless, these results suggest that low operating voltage OFETs, enabled using high-k dielectrics, benefit from reduced hysteresis and increased stability during operation as well as lower power dissipation.

Several groups have also analyzed the effects of the thickness of Al_2O_3 gate dielectrics. Lim et al. fabricated and compared pentacene-based OFETs on a polyethersulfone (PES) substrate with different thicknesses of Al_2O_3 dielectric (80, 120, and 150 nm) grown at 150 °C by PEALD.[88] For the 80 nm thick device, they did not observe electrical response, probably due to the existence of leaky and weak points in the dielectric resulting from its low thickness. The best results ($\mu = 0.62$ $cm^2 V^{-1} s^{-1}$, $V_T = -1.2$ V, $I_{ON}/I_{OFF} = 10^7$) were found for the 150 nm thick dielectric (Figure 12). The authors argued that the improvement was due to the surface morphology and that it was necessary for the gate insulators to be sufficiently thick to obtain satisfactory device performance in pentacene devices on PES substrates. They suggested that their 150 nm thick Al_2O_3 (by PEALD) was sufficiently thick and compact to overcome the difficulties that usually arise using plastic substrates. Finally, Song et al. studied different nanometer thick Al_2O_3 dielectrics by changing the conditions of an oxygen plasma growth process.[89] A 5 nm thick dielectric layer (10 s oxygen plasma treatment) exhibits a leakage current of $\sim 10^{-7}$ A cm^{-2}, a capacitance of 1.1×10^{-6} F cm^{-2}, and a breakdown field of 3 MV cm^{-1}, comparable to the same metal oxide grown by RF magnetron sputtering[80] but lower than thermally grown SiO_2.[90] The authors argued that the transport mechanism in these very thin layers appears to be direct tunneling in a voltage region from 0 to 0.5 V, because the current density J was found to be proportional to the applied voltage. For higher voltages, Fowler−Nordheim tunneling was the dominant transport mechanism because $\ln(J/V^2)$ is proportional to $-1/V$. Optimum results ($\mu = 0.10$ $cm^2 V^{-1} s^{-1}$, $V_T = -1.12$ V, $I_{ON}/I_{OFF} = 10^3$) were obtained for thicker dielectric films (20 s oxygen plasma treatment) due to the reduction in leakage current.

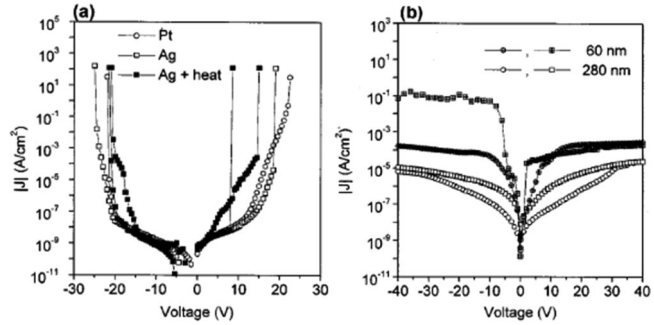


Figure 13. Electrical characteristics of Ta_2O_5 dielectrics formed by anodization. Figures a and b show leakage currents as a function of voltage for both anodized Ta_2O_5 (∼50 nm) and SiO_2 (∼60 and ∼280 nm) dielectric films, respectively. Capacitor structures of Ta_2O_5 were tested with Pt and electroless silver (untreated and heat-treated at 150 °C for 1 h) top contacts. Reprinted with permission from ref 91. Copyright 2000 American Chemical Society.

In summary, all of the results discussed in this section on Al_2O_3 gate dielectrics indicate that, even if the dielectric constant of this metal oxide is not very high ($k \approx 8$), it is nevertheless a good candidate to simultaneously ensure low operating voltages and device high stability. Very high-k materials frequently lack stability while allowing very low-voltage operation, whereas low-k materials offer low leakage currents and high stability but require higher operating voltages.

3.1.2. Tantalum Oxide

Anodized Ta_2O_5 ($k \approx 23$) was used for the first time by Katz et al.[91] to demonstrate the solution-based fabrication of OFETs with microcontact printed electrodes (∼1 μm). Through anodization, they obtained high-quality dielectric oxide layers with electrical leakages lower than 10^{-8} A/cm^2 at 1 MV/cm (for a ∼50 nm thick film) and breakdown fields between 4 and 5 MV/cm (see Figure 13). Both n- and p-channel organic transistors were fabricated using copper hexadecafluorophthalocyanine ($F_{16}CuPc$) and dihexyl quinquethiophene (DHα5T), respectively, demonstrating the compatibility of this dielectric with both n- and p-type organic semiconductors and with flexible plastic substrates. They found that devices with top contact configurations perform better than the ones with bottom contacts in the 2−6 V range.

Subsequently, Bartic et al.[92] deposited Ta_2O_5 thin film dielectrics of varying thicknesses by electron-beam evaporation. This method appears to be suitable for plastic electronics due to the relatively low temperatures required. The dielectric exhibits leakages currents of $\sim 10^{-7}-10^{-8}$ A/cm^2 at 0.5 MV/cm, depending on the transistor configuration, breakdown strengths higher than 1 MV/cm, and a dielectric constant of ∼21. These authors fabricated transistors both in staggered and in inverted staggered configurations using poly(3-hexylthiophene) (P3HT) as the semiconductor and reported mobilities of 0.004 and 0.02 $cm^2 V^{-1} s^{-1}$, respectively. Oxygen doping was detected when the Ta_2O_5 films were deposited on top of the organic layer, and this altered the device performance.

In 2003, Iino et al.[93] fabricated room-temperature anodized Ta_2O_5 dielectrics using Ta on polycarbonate substrates as the FET gate electrode. The gate insulators were fabricated as stacked structures of aluminum and tantalum to avoid Ta film cracking. Derived capacitance values ranged from 109 to 248 nF cm^{-2} for dielectrics with thicknesses of 86−188

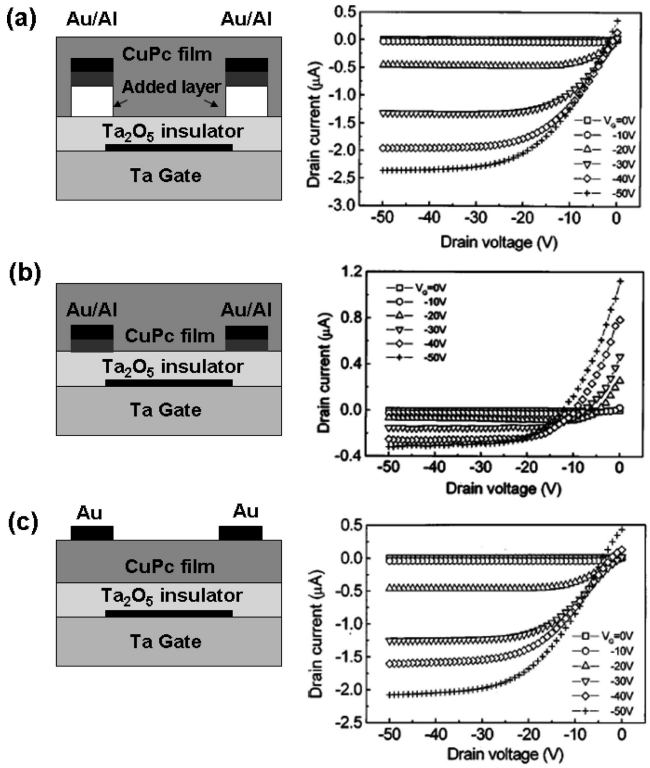


Figure 14. Schematic structures and output characteristics of the OFET devices with the following structures: (a) structure reported in ref 94, (b) bottom-contact structure, and (c) top-contact structure. Reprinted with permission from ref 94. Copyright 2003 American Institute of Physics.

nm ($k \approx 23-27$). Pentacene-based OFETs showed a mobility of 0.36 $cm^2\ V^{-1}\ s^{-1}$ in the voltage range of 5 V. The same year, Yuan et al.[94] reported a method to fabricate copper phthalocyanine (CuPc) bottom-contact devices with low leakage currents using a low-dielectric polymer, poly(methylmethacrylate) (PMMA), between the magneton sputtered Ta_2O_5 insulator and source/drain electrodes. With this device structure, leakage currents were reduced from 1.1×10^{-6} to 3.5×10^{-7} A at $V_G = -50$ V, and mobilities of 0.01 $cm^2\ V^{-1}\ s^{-1}$ were obtained, 1 order of magnitude higher than for bottom-contact devices without the PMMA layer, and almost the same as that for the top-contact device (Figure 14).

In 2003, Inoue et al.[95] characterized organic thin-film transistors based on anthracene oligomers on Si/SiO_2 substrates, obtaining the highest mobility of 0.13 $cm^2\ V^{-1}\ s^{-1}$ for 6−6′-dihexyl-[2−2′]bianthracene. The optimization of these device characteristics and lowering of the operating voltage were possible by using anodically oxidized 130 nm thick Ta_2O_5 gate insulators, obtaining a field-mobility of 0.22 $cm^2\ V^{-1}\ s^{-1}$ and a current on/off ratio of 10^6. In the case of anodized insulators, the characteristics of the anodized film are affected by the electrolyte solution and by the anodization conditions.[96] With this in mind, Fujisaki et al.[97] analyzed the characteristics of pentacene-based OFETs on plastic substrates using different electrolyte solutions (phosphoric acid and ammonium borate) to grow the anodized Ta_2O_5 film. They reported that when ammonium borate is used instead of phosphoric acid, the FET device characteristics are significantly improved, with a mobility of 0.51 $cm^2\ V^{-1}\ s^{-1}$, I_{ON}/I_{OFF} of 10^5, and V_T of −1.1 V at a low drain voltage of 3 V (Figure 15). They argued that the phosphoric acid solution introduces impurities at the dielectric/semiconductor interface. A smoother surface is also found by AFM when using ammonium borate as the electrolyte (see Figure 15).

Ohta et al.[98] fabricated pentacene-based transistors for switching organic light-emitting diodes. The devices were bottom contact structures with the Ta_2O_5 gate dielectric layers produced by anodization in ammonium adipate solution. The OFET mobility of the corresponding device was increased from 0.038 to 0.20 $cm^2\ V^{-1}\ s^{-1}$ by treating the dielectric surface with HMDS. The authors argued that this improvement was due to better molecular organization, morphology, and ordering of the pentacene. The same HMDS-treatment was also used on an anodized e-beam evaporated Ta film by Jeong et al.,[99] resulting in a gate leakage current reduction by more than 70%. The mobility of pentacene-based transistors was also increased from 0.45 $cm^2\ V^{-1}\ s^{-1}$ on untreated Ta_2O_5 dielectrics ($C = 325$ nF cm^{-2}) to 0.51 on HMDS-treated Ta_2O_5 ($C = 245$ nF cm^{-2}), due to increased pentacene grain size. Exactly how the HMDS molecules bind to the dielectric surface is not clear, but the authors suggest chemisorptive reaction with surface hydroxyl groups incorporated into the Ta_2O_5 during the anodization.

More recently, Yu et al.[100] optimized vacuum-evaporated vanadyl-phthalocyanine (VOPc) semiconducting films using Ta_2O_5 gate dielectrics among others. The Ta_2O_5 dielectric (∼500 nm in thickness, $C \approx 35$ nF cm^{-2}) was deposited by magnetron sputtering. Using a high substrate temperature (150 °C) and a low deposition rate, they observed larger and more regular, closely packed VOPc terraced grains than those achieved using a thermally grown SiO_2 gate dielectric, measuring mobilities of 0.05−0.1 $cm^2\ V^{-1}\ s^{-1}$ (vs 0.04−0.06 $cm^2\ V^{-1}\ s^{-1}$ on SiO_2). In 2008, Deman et al.[101] analyzed the effect of different Ta_2O_5 deposition methods on pentacene growth and, consequently, on device performance. They observed improved FET performance parameters for an e-beam evaporated Ta_2O_5 film as compared to an anodized film. They ascribed this result to the more hydrophobic surface of the evaporated dielectric, arguing that wettability is an important parameter governing pentacene grain size.

3.1.3. Titanium Dioxide

TiO_2 ($k = 41$) was used for the first time by G. Wang and co-workers[45c] in regioregular poly(3-hexylthiophene)-based OFETs, obtaining a carrier mobility of 5×10^{-3} $cm^2\ V^{-1}\ s^{-1}$ at low drive voltages (∼2 V). This mobility value is reduced from that obtained with SiO_2 (200 nm thick) by more than a factor of 20×,[102] implying increased disorder and surface roughness at the dielectric−semiconductor interface. In this study, the insulator layer was deposited using a wide-area rf-biased, pulsed dc linear scanning magnetron physical vapor deposition process. This dielectric also exhibited a relatively large leakage current that limited the on/off ratio to 10^2. The deposition of a thin SiO_2 layer (17 nm) on top of the TiO_2 decreased the capacitance from 373 nF/cm^2 ($k = 41$) to 143 nF/cm^2 ($k_{eff} = 19$), but also decreased the leakage current by a factor of $\sim 10^2$, and yielded better device performance (5.4×10^{-2} $cm^2\ V^{-1}\ s^{-1}$, $I_{ON}/I_{OFF} \approx 10^4$); this value of mobility is within a factor of 2−4 of the best values obtained for P3HT (poly-3-hexylthiophene) OFETs on SiO_2.[102,103]

Majewski et al. fabricated pentacene and poly(triarylamine) (PTTA) OFETs using anodized TiO_2 as the gate dielectric.[104,105] The high dielectric constant of this metal oxide allowed the transistors to operate in a voltage range below 1 V, exhibiting

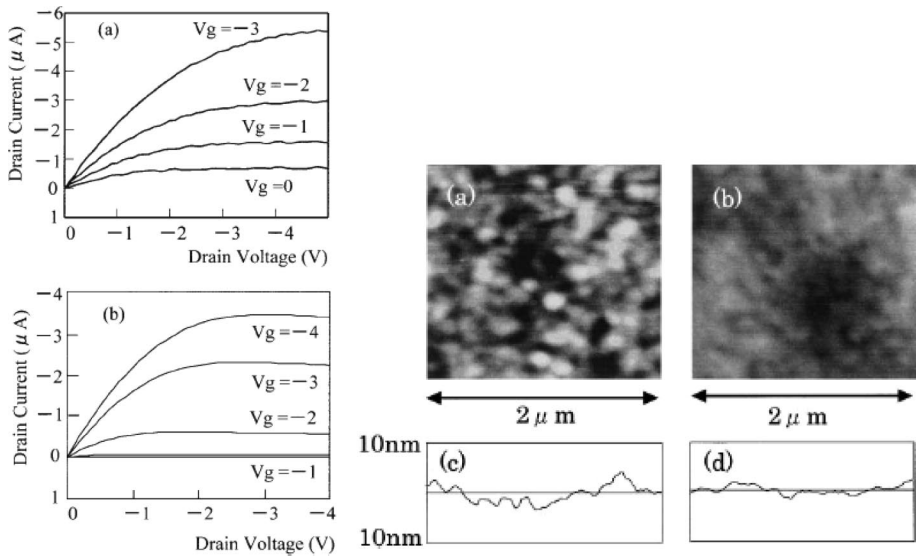


Figure 15. (Left) Output characteristics of OFETs with an anodized Ta_2O_5 gate insulator using (a) phosphoric acid and (b) ammonium borate in the aqueous anodization electrolyte. (Right) Surface morphology of anodized Ta_2O_5 using (a) phosphoric acid and (b) ammonium borate. Parts (c) and (d) show the horizontal cross sections of films (a) and (b), respectively. Reprinted with permission from ref 97. Copyright 2004 Japan Society of Applied Physics.

mobilities of 0.15 and $<10^{-5}$ cm^2 V^{-1} s^{-1} for pentacene and PTTA devices, respectively. More recently, Ramajothi et al.[106] demonstrated a room-temperature solution process to fabricate OFETs based on regioregular-P3HT. The dielectric material (TiO_2) was prepared by a sol−gel technique, the gate insulator layer was deposited by spin-coating, and the semiconductor films were fabricated by drop-casting. The spin-coated TiO_2 had an amorphous microstructure ($k = 27$), yielding field-effect mobilities of 3.73×10^{-3} cm^2 V^{-1} s^{-1} and V_T of 3 V for the regioregular-P3HT-based device. Very low FET I_{ON}/I_{OFF} ratios ($\sim 10^1$) were obtained by this process. The authors proposed that annealing of the gate layer should improve the performance by the crystallization of the TiO_2. Bulk TiO_2 in the rutile phase exhibits a k value of $\sim$100.[107]

As observed above, one of the principal drawbacks of TiO_2 dielectric films that limits their use in OFETs is high leakage current. Some strategies used in inorganic devices to suppress this leakage current have been used for the fabrication of cryogenic devices using high-k sol−gel-derived TiO_2 electron beam resists.[108] In this case, at liquid helium temperatures, the leakage current is suppressed, and acceptable FET behavior is achieved.

In 2008, Cai et al.[109] fabricated oleic acid-capped TiO_2 (AO-TiO_2) core−shell nanoparticles, which exhibited good dielectric properties after deposition by spin-coating. The dielectric films showed a dielectric constant of $\sim$5.3 and low leakage current of $\sim 3 \times 10^8$ A/m^2 under an electric field of 1 MV/cm. The authors fabricated OFETs using both poly(3,3‴-didodecylquaterthiophene) and pentacene as the semiconducting materials and reported mobilities of 0.05 and 0.2 cm^2 V^{-1} s^{-1}, respectively, with $I_{ON}/I_{OFF} = 10^3-10^5$. This dielectric material thus appears to be a good candidate for printable OFETs.

3.1.4. Hafnium Dioxide

HfO_2 thin films have been widely investigated as potential high-k oxides to replace SiO_2 in future silicon microelectronics[110] because they offer a high dielectric constant, close to that of Ta_2O_5 ($k \approx 22-25$), but with a larger band gap. However, HfO_2 gate dielectrics were not implemented in organic-based devices until 2007. In that year, Tardy et al.[111] proposed two different methods of depositing an HfO_2 dielectric layer on top of highly doped Si-p^{+2} substrates, sol−gel deposition and an anodization process. Pentacene-based OFETs with anodized HfO_2 dielectric layers operate at voltages as low as 1 V, exhibiting a mobility of 2.2×10^{-2} cm^2 V^{-1} s^{-1} and a V_T of −0.75 V. However, these devices have two weak points: hysteresis and a lower mobility than that usually observed for the same semiconductor on other anodized high-k dielectrics.[81b,93] The authors ascribed the latter behavior to a poorly organized pentacene−HfO_2 interface,[101] arising from surface roughness. In contrast, devices fabricated with nanoporous sol−gel dielectric layers ($k = 11$) exhibited acceptable performance, with mobilities up to 0.13 cm^2 V^{-1} s^{-1}, $I_{ON}/I_{OFF} \approx 5 \times 10^{-3}$, and V_T of −0.3 V at an operating voltage of about 1 V. The lower leakage currents as compared to the anodized films may be due to the existence of a thin SiO_2 layer resulting from a postdeposition annealing process at 450 °C. This annealing step, on the other hand, renders this process incompatible with plastic substrate technologies.

Cho et al.[112] analyzed pentacene-based thin film transistors with 6 nm thick $(HfO_2)_x(SiO_2)_{1-x}$ ($x = 0.25$ and 0.75) gate dielectrics and found different device response characteristics depending on the composition of the insulator. They found that devices with a $(HfO_2)_{0.75}(SiO_2)_{0.25}$ gate insulator exhibited a higher saturation drain current, which could be explained considering the higher capacitance of the dielectric layer. In contrast, in the device with $(HfO_2)_{0.25}(SiO_2)_{0.75}$, the gate insulator induced a lower threshold voltage. Using in situ UPS experiments, the authors related this effect to the larger work function of the latter dielectric. Measured mobilities for both OFETs were the same at 0.11 cm^2 V^{-1} s^{-1} in a voltage range of −4 V.

Also using pentacene and a double stack dielectric layer, Wu et al.[113] fabricated a thin film transistor with a structure different from the one conventionally employed for OFETs. In this structure, they deposited the pentacene layer directly onto Si and then sputtered on HfO_2 and Si_3N_4 dielectric layers ($k = 10.4$) to lower the operating voltage with respect to

SiO_2 and to reduce gate leakage current. This configuration allowed an acceptable carrier mobility of 0.21 $cm^2\ V^{-1}\ s^{-1}$, a V_T of −7 V, and improved the lifetimes of the devices as compared to conventional OFETs.

3.1.5. Zirconium Dioxide

Despite the high dielectric constant of ZrO_2 ($k \approx 25$), few reports have appeared using this metal oxide alone as the insulator layer in organic devices, probably due to its poor compatibility with typical organic materials. Using ZrO_2 as the gate dielectric, Havey et al.[114] reported the integration of thin films (∼8 nm) of this metal oxide into single-walled carbon nanotube (SWNT) transistors by an atomic-layer deposition (ALD) growth process. Using this process, they obtained dielectric layers with negligible tunnelling leakage current in voltage range below 3 V and achieved high-performance p- and n-type devices.

In 2004, Kim et al.[115] reported the fabrication of pentacene-based OFETs with ZrO_2 gate dielectrics, measuring a field-effect mobility of 0.12 $cm^2\ V^{-1}\ s^{-1}$ and I_{ON}/I_{OFF} of 10^4 in a voltage range of −30 V. However, they observed serious device degradation, which they attributed to an increased surface potential barrier height between the pentacene and the gate dielectric layer. Furthermore, irregular pentacene grains are formed under these conditions due to the weak cohesive interaction between the semiconductor and the dielectric. This problem was solved by functionalizing the metal oxide dielectric surface with an organic SAM (OTMS, octadecyltrimethoxysilane), achieving reduction of the surface defect density and improved semiconductor growth. An increase in pentacene mobility from 0.12 to 0.66 $cm^2\ V^{-1}\ s^{-1}$ and I_{ON}/I_{OFF} from 10^4 to 10^5 was achieved by the organic surface treatment.

3.1.6. Cerium Dioxide

Cerium dioxide, with a dielectric constant of ∼23, has appeared as a promising dielectric layer candidate in inorganic electronics.[116] However, its performance in organic devices is poor due to its polycrystalline structure,[117] which increases leakage current. Grain boundaries in polycrystalline structures usually serve as efficient leakage pathways, causing irreversible degradation in OFETs. As a possible solution, some authors have investigated the suitability of CeO_2-SiO_2 composite films; even if the capacitances are lower, these films are amorphous as well as denser and smoother than bare CeO_2 films.[118] Nevertheless, additional treatments are required (i.e., surface modification with organic groups) to achieve low leakage currents and acceptable pentacene grain growth.[118,119]

Other metal oxides have been investigated to a lesser extent. For example, Kang et al.[120] used ion beam-assisted deposited (IBAD) techniques to grow Gd_2O_3 layers as gate dielectrics for pentacene OFETs. These dielectric layers offer a dielectric constant smaller ($k \approx 7.4$) than that previously reported for the same metal oxide,[121] due to the presence of the amorphous phase, but this decreases the V_T to −3.5 V, significantly smaller than that obtained with SiO_2 ($V_T \approx 13-15$). The devices exhibit a moderate pentacene mobility of 0.1 $cm^2\ V^{-1}\ s^{-1}$ due to the small size of pentacene grains on the Gd_2O_3 dielectric. Finally, it is of interest to comment on the contribution of de Boer et al.,[122] where single-crystal OFETs (tetracene, rubrene, and pentacene) were fabricated with various metal oxides as dielectric layers (Ta_2O_5, ZrO_2, and SiO_2). The results indicate that leakage currents greater than 10^{-9} A cm^{-2} flowing through the gate insulator cause irreversible device degradation, independent of the semiconductor and dielectric used. That result indicates that a significant effort will be required to optimize insulator electrical properties if stable single-crystal OFETs are to be fabricated.

Table 1 summarizes the properties of various inorganic gate dielectrics.

3.2. Organic Dielectrics

3.2.1. Polymer Dielectrics

The first successful attempt to use polymeric organic materials as gate insulator layers in OFETs was reported by Peng et al. in 1990.[123] They fabricated devices using a variety of organic polymer insulators and evaporated α-sexithienyl (α6T) films on top as the semiconductor. Their results indicated a strong correlation between the field-effect mobility and the dielectric constant of the insulator, finding no field-enhanced current in the case of low k polymers such as polymethylmethacrylate (PMMA; $k \approx 3.5$) and polystyrene (PS; $k \approx 2.6$). In contrast, good results were obtained for polyvinyl alcohol (PVA; $k \approx 7.8$) and cyanoethylpullulan (CYEPL; $k \approx 18.5$), even surpassing the field-effect mobility obtained with SiO_2-based devices in the case of CYEPL. Using polyvinyl chloride (PVC; $k \approx 4.6$) yielded irreproducible results. Encouraged by these results, Peng et al. fabricated the first all-organic electronic device (except for the electrical contacts), using α6T as the semiconductor, CYEPL as the gate dielectric, and poly(parabanic acid) resin (PPA) as the FET substrate. They observed mobilities of 4.3 × 10^{-1} $cm^2\ V^{-1}\ s^{-1}$ and appreciable mechanical flexibility.[124] Later, an all-organic printed device was fabricated,[125] using a polymeric graphite-based ink to create the contacts, polyester as the gate dielectric, vapor-deposited dihexylsexithiophene (DH-6T) as the semiconductor, and adhesive tape as the substrate. Mobilities of 6 × 10^{-2} $cm^2\ V^{-1}\ s^{-1}$ and improved mechanical properties were reported.

Bao et al.[126] went a step further and fabricated a regioregular poly(3-hexylthiophene)-based transistor where all of the essential components were printed directly onto a plastic substrate. They selected an ITO-coated poly(ethylene terephthalate) film as the substrate, a polyimide layer as the gate dielectric ($C \approx 20$ nF cm^{-2}), and a conductive ink for the contact electrodes, resulting in OFETs with mobilities between 0.01 and 0.03 $cm^2\ V^{-1}\ s^{-1}$. In 1998, Drury et al.[127] fabricated an all-polymer integrated circuit in a top-gate configuration using polythienylenevinylene (PTV) as the semiconductor and polyvinylphenol (PVP) as the gate dielectric. The choice of this semiconductor, despite its low field-effect mobility (∼5 × 10^{-5} to 10^{-3} $cm^2\ V^{-1}\ s^{-1}$), was due its compatibility with top-gate OFET structures. A few years later, Gelinck et al.[128] solved this problem using a bottom-gate structure. They obtained field-effect mobilities of 10^{-2}, 3 × 10^{-3}, and 10^{-3} $cm^2\ V^{-1}\ s^{-1}$ for pentacene, P3HT, and PTV, respectively, using a spin-coated 300 nm thick commercially available photoresist as the gate insulator.

Sirringhaus et al. for the first time fabricated organic transistors using an inkjet printing technique.[129] They were successful in defining source and drain electrodes by spreading the conducting polymer ink (PEDOT:PSS) on a patterned (hydrophobic−hydrophilic) surface. TFT devices were fabricated in a top-gate configuration by spin-coating the

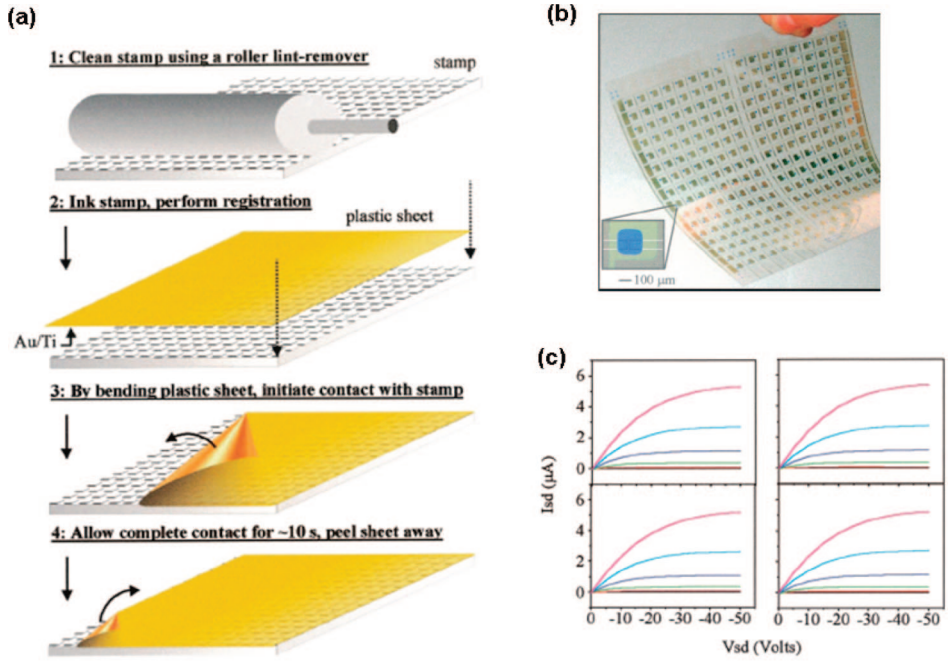


Figure 16. (a) Procedure for using μCP to pattern over large areas. (b) Image of a completed plastic active matrix backplane circuit (inset: optical micrograph of a transistor). (c) Output plots of several transistors in the plastic backplane circuit. Reprinted with permission from ref 132. Copyright 2001 National Academy of Sciences.

poly(9,9-dioctylfluorene-*co*-bithiophene) (F8T2) semiconductor followed by spin-coating of a PVP gate dielectric, and inkjet-printing the PEDOT/PSS gate electrode. The devices exhibit a field-effect mobility of 0.01−0.02 $cm^2\ V^{-1}\ s^{-1}$ and an I_{ON}/I_{OFF} ratio of 10^5.

The first printed organic device that involved multiple transistors with micrometer-sized features was fabricated by Rogers et al.[130] The configurations of the devices were bottom-contact. A patterned ITO layer on a sheet of poly(ethylene terephthalate) (PET) was used as the gate for the transistors and a preimidized polyimide as the dielectric layer. The thickness of the dielectric was ~2 μm, and the capacitance was ~1 nF cm^{-2}. Source and drain electrodes were deposited by electron beam evaporation of a 20 nm thick gold films, followed by a microcontact printing (μCP) and subsequent etching.[131] In this procedure, a rubber stamp delivers an ink to selected regions of the gold surface, which forms a hexadecanethiol SAM. Next, an aqueous etchant removes the gold that is not protected by the SAM, defining source and drain electrodes. Finally, the authors removed the printed SAM by exposing it to ultraviolet light. The complementary inverted circuits were completed by shadow mask evaporation of p-type α-sexithiophene (α-6T) and n-type $F_{16}CuPc$ semiconductors. Mobilities were ~0.01 and ~0.001 $cm^2\ V^{-1}\ s^{-1}$, respectively. The same group also demonstrated the fabrication of organic active-matrix backplane circuits composed of 256 transistors for large mechanically flexible "electronic" paper, based on microencapsulated electrophoretic inks and microcontact printing (μCP) to pattern large areas, as shown in Figure 16a and b.[132] By this method, they were able to fabricate circuits having good device uniformity as can be seen in Figure 16c, where the output plots for four different devices are shown. This group used an organosilsesquioxane spin-on glass as the dielectric material. This insulator was chosen because: (i) thin films (<1 μm) show low electrical leakage, (ii) it can be cured at low (<150 °C) temperatures, (iii) it is chemically compatible with a range of organic semiconductors, and (iv) it can be used with etchants for μCP. The capacitance of the films (0.8−1.0 μm) was between 2 and 10 nF cm^{-2}. A batch of semiconductors (n-type and p-type) was tested in this configuration, exhibiting mobilities comparable to those observed previously with SiO_2 dielectrics. Ambient FET stability was increased by encapsulation of the devices.

In a following paper by Rogers et al., different commercially available silsesquioxane polymers were tested as dielectrics using six p- and n-channel semiconductors.[133] Among the glass resins studied, optimum results were found for the ones with methyl and phenyl pedant groups (GR 150), which were suggested to be related to better compatibility of the conjugated semiconducting materials with the phenyl-rich surface. Furthermore, superior glass resin films were obtained when the silicon substrates were first treated with an oxygen plasma, which enhanced the wettability and adhesion of the glass resins. This group also examined the effects of surface treatment with a number of silane reagents and of different configurations, both top and bottom contact OFETs.

In 2002, Kim et al. used a photoacrylic polymer as the dielectric layer and pentacene as the semiconductor to fabricate thin film transistors with mobilities up to 0.075 cm $V^{-1}\ s^{-1}$, V_T of −6 V, and I_{ON}/I_{OFF} of 10^6.[134] They found dendritic pentacene growth with large grains on the photoacrylic film due to its hydrophobic character, indicating that further steps such as SAM deposition (e.g., OTS) were not required to enhance the device performance. In a following paper,[135] they reported an organic electrophosphorescent device driven by all-organic pentacene field-effect transistors with a 0.5 μm thick photoacrylic gate dielectric layer. They obtained field-effect mobilities up to 0.13 $cm^2\ V^{-1}\ s^{-1}$.

This same year, Halik et al. fabricated fully patterned all-organic FETs using spin-coated poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid (PEDOT:PSS) as contact electrodes, spin-coated poly-4-vinylphenol (PVP) as the gate dielectric layer, and pentacene or poly-3-hexylthiophene as the active semiconductor layer.[136] For the

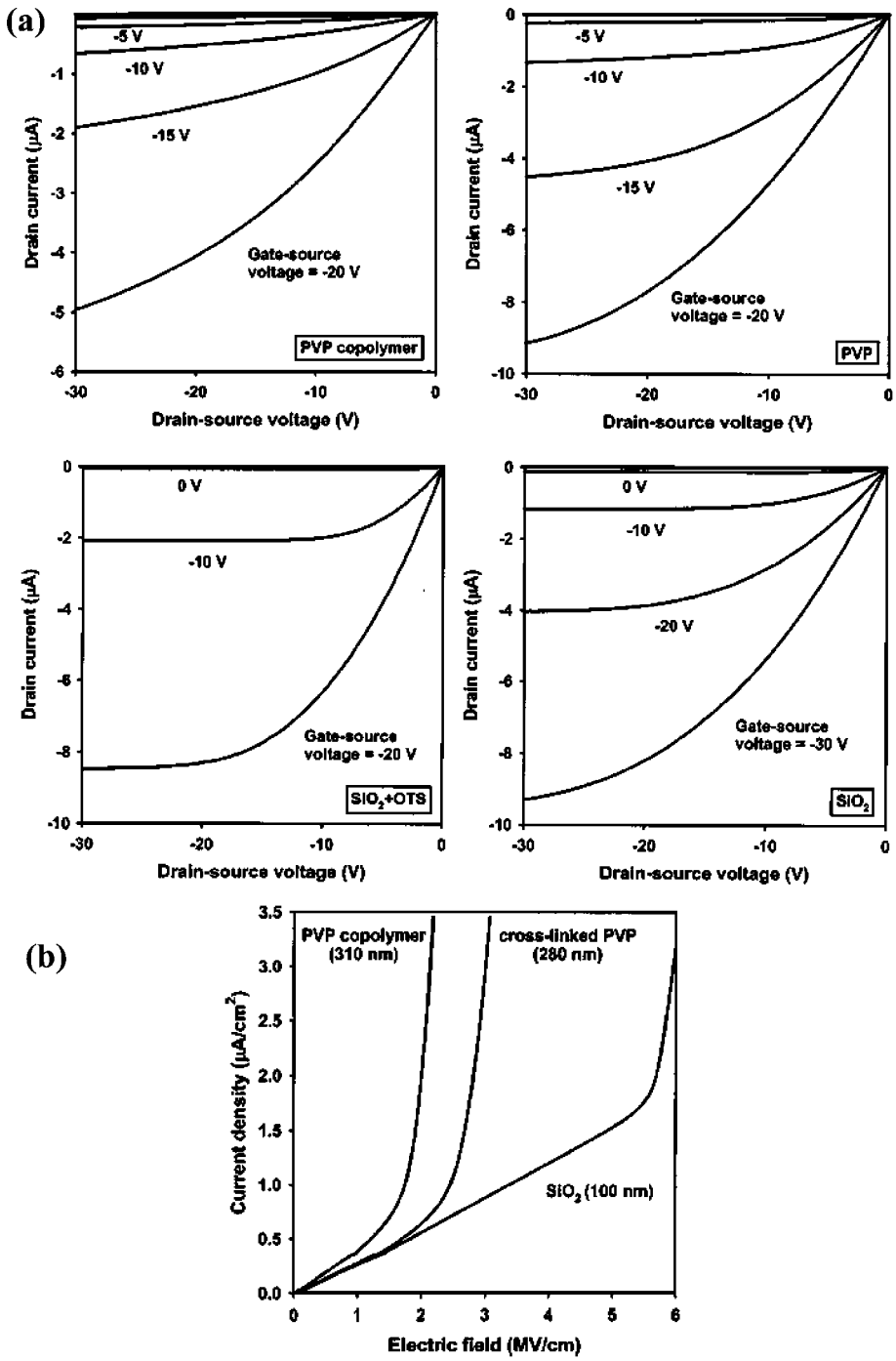


Figure 17. (a) Electrical output characteristics of pentacene OFETs with different gate dielectrics. (b) Current leakage through three different gate dielectric films. Reprinted with permission from ref 137. Copyright 2002 American Institute of Physics.

pentacene devices, they reported carrier mobilities as large as 0.1 $cm^2\ V^{-1}\ s^{-1}$, similar to the ones obtained using thermally grown SiO_2, but with lower I_{ON}/I_{OFF} values (10^3 vs 10^6, polymeric vs SiO_2) and a larger (worse) subthreshold slope (5 V/decade vs 0.7 V/decade). Nonetheless, these were the largest carrier mobilities reported to that date with polymeric source and drain contacts. Using poly-3-hexylthiophene, they measured hole mobilities of 0.002 $cm^2\ V^{-1}\ s^{-1}$ and I_{ON}/I_{OFF} values of 10^2, similar to performance obtained with inorganic gate dielectrics and metal contacts. These results indicated the possibility of substituting inorganic materials with polymers in the fabrication of OFETs and achieving similar electrical performance. Furthermore, in a following paper, the same group demonstrated improved electrical performance of pentacene-based OFETs using two different spin-coated polymer gate dielectrics, a cross-linked poly-4-vinylphenol (cross-linked PVP) and a poly-4-vinylphenol-*co*-2-hydroxyethylmethacrylate PVP copolymer, with thicknesses ranging from 260 to 380 nm.[137] These two dielectrics were compared to thermally grown SiO_2 dielectrics, with and without OTS treatment. The gate dielectric leakages for these polymer films were similar to the leakage currents observed for a SiO_2 dielectric layer (Figure 17b).

The electrical characteristics of the above pentacene devices (see Figure 17) indicate an increase of the carrier mobility from 0.4 and 1.0 $cm^2\ V^{-1}\ s^{-1}$ for the SiO_2 and OTS-treated SiO_2, respectively, to 3 $cm^2\ V^{-1}\ s^{-1}$ for the polymer dielectrics. Nevertheless, it is important to note that FETs fabricated with these polymeric gate dielectrics exhibit substantial hysteresis as compared to those fabricated with

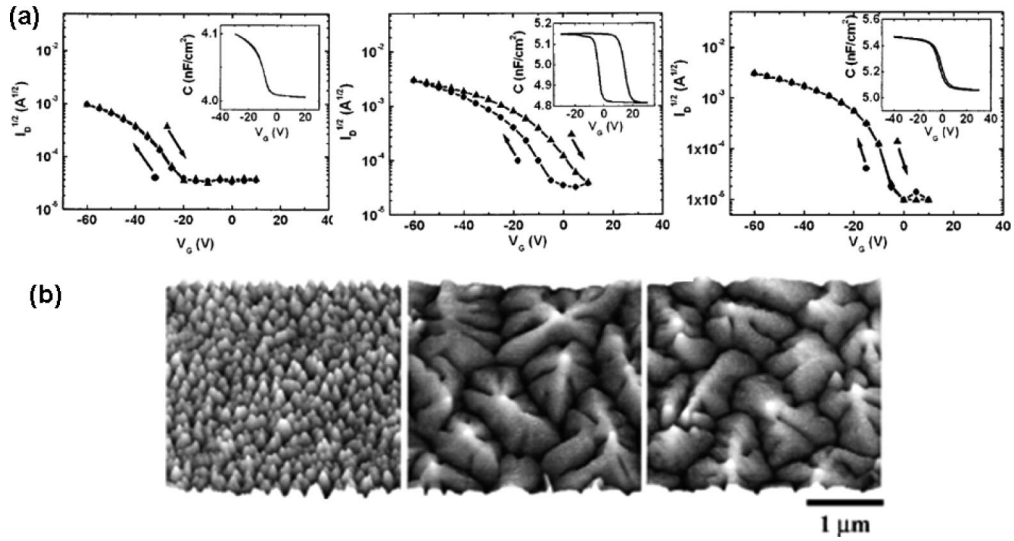


Figure 18. (a) Plot of pentacene FET $I_D^{1/2}$ vs V_G for a fixed V_D of −50 V for PVP, PVAc, and PVAc−PVP bilayer dielectrics (from left to right). The insets are C vs V_G characteristics at an ac frequency of 100 kHz. (b) AFM images of pentacene films on PVAc, PVP, and PVAc−PVP bilayer (from left to right). Reprinted with permission from ref 140. Copyright 2004 American Institute of Physics.

inorganic insulators. Using the cross-linked polymer, all-organic OFETs and inverters were fabricated, substituting the inorganic metal contacts with the conducting polymer PEDOT doped with PPS.[138] Furthermore, the effects of substituting the inorganic dielectric or the contacts with polymeric materials were analyzed independently by the fabrication of different test structures on heavily doped silicon wafers, indicating no sacrifice of device performance. The robustness of the polymeric dielectric was also demonstrated by the fabrication of fully patterned transistors on glass and on flexible polymeric substrates, an advance essential to integrating OFETs into circuits and displays.

Later, Parashokov et al. reported a strong correlation between the dielectric constant of the insulator, the solvent used for the dielectric deposition, and the organic field-effect mobility. They used as dielectric materials PVP, PVA, and CYEPL, and as the semiconductor, poly(3-butylthiophene).[139] They produced all-organic FETs on flexible polyimide substrates and obtained carrier mobilities as large as 0.04 $cm^2\ V^{-1}\ s^{-1}$ in the case of the CYEPL dielectric. The lower mobilities found for the PVP-based transistors were attributed to the roughness of this polymer film (∼29 nm).

One major problem presented by PVP, which has been the most heavily used polymer dielectric to date, is the substantial hysteresis that shifts the threshold voltage. In 2004, Park et al. addressed this problem by using a bilayer dielectric in which two dielectrics act cooperatively to enhance device performance.[140] They found that in an OFET with a bilayer dielectric of 1 μm polyvinylacetate (PVAc) and 20 nm PVP, the electrical properties of the pentacene semiconductor are largely determined by the PVP dielectric layer in contact with the semiconductor ($\mu \approx 0.1\ cm^2\ V^{-1}\ s^{-1}$), but that the dielectric properties are determined by the thick PVAc dielectric, leading to reduced hysteresis (see Figure 18a). AFM measurements showed that the pentacene grains formed on PVAc are relatively small, whereas in both PVP and the bilayer structure, large dendritic grains are formed (Figure 18b). This may explain the reason for the higher carrier mobility in the pentacene films. In addition, by comparing the response of the OFETs fabricated from the single- and double-layer dielectrics, Park et al. concluded that hysteresis is due to a bulk phenomenon rather than to interface effects.

In 2004, Sandberg et al. proposed the concept of a HIFET (hygroscopic insulator field-effect transistors) where enhancement of the electronic properties of P3HT is observed when the device is exposed to moisture.[141] The dielectric used was PVP with a thickness of ∼1.2 μm and a capacitance of 4.3 nF cm^{-2}. The capacitance increases depend on the relative humidity and time of ambient exposure. These HITFTs exhibit good performance in contact with fumes of small and polar solvents, but exhibit minimal current modulation with large and nonpolar molecules. The authors explained the current enhancement by the presence of ions (presumably residual contaminants arising from the synthesis), which induce ionic processes at the moisturized gate dielectric−semiconductor interface. Thus, the hygroscopic insulator and the presence of a solvent are essential for HIFET operation.

In all of the above examples, the polymers were limited to a thickness of ≥300 nm to obtain pinhole-free films. In 2004, for the first time, Chua et al. reported a siloxane-based material, divinyltetramethyldisiloxane-bis(benzocyclobutene) (BCB), that forms defect-free films down to a few tens of nanometers by simple solution-casting.[37] This dielectric is obtained via thermal ring-opening and successive 4 + 2 Diels−Alder cycloaddition/polymerization of the BCB monomer, and exhibits a very high dielectric breakdown strength (>3 MV/cm), low leakage current (<10 nA), and low fixed-charge and trap densities in the bulk and at interfaces. The corresponding devices fabricated using poly(9,9-dialkylfluorene-*alt*-triarylamine) as the semiconductor and PEDOT:PSSR (where R = hexadecyltrimethylammonium) as the gate electrode display mobilities of few $10^{-4}\ cm^2\ V^{-1}\ s^{-1}$ and remarkable stability with temperature and time.

In 2004, a new method for fabricating polymeric insulators was reported by Rutenberg et al.[142] They used surface-initiated ring-opening metathesis polymerization (SI-ROMP) as a method of growing polynorbornene dielectric layers of tailored thickness, simply by varying the polymerization conditions. Devices fabricated using pentacene and a ∼1.2 μm dielectric layer ($C \approx 3$ nF cm^{-2}) exhibited mobilities and I_{ON}/I_{OFF} of 0.1−0.3 $cm^2\ V^{-1}\ s^{-1}$ and 10−100, respectively, and exhibited little hysteresis. In this report, they demonstrated that surface-initiated polymer dielectric layers are both chemically and electrically compatible with other

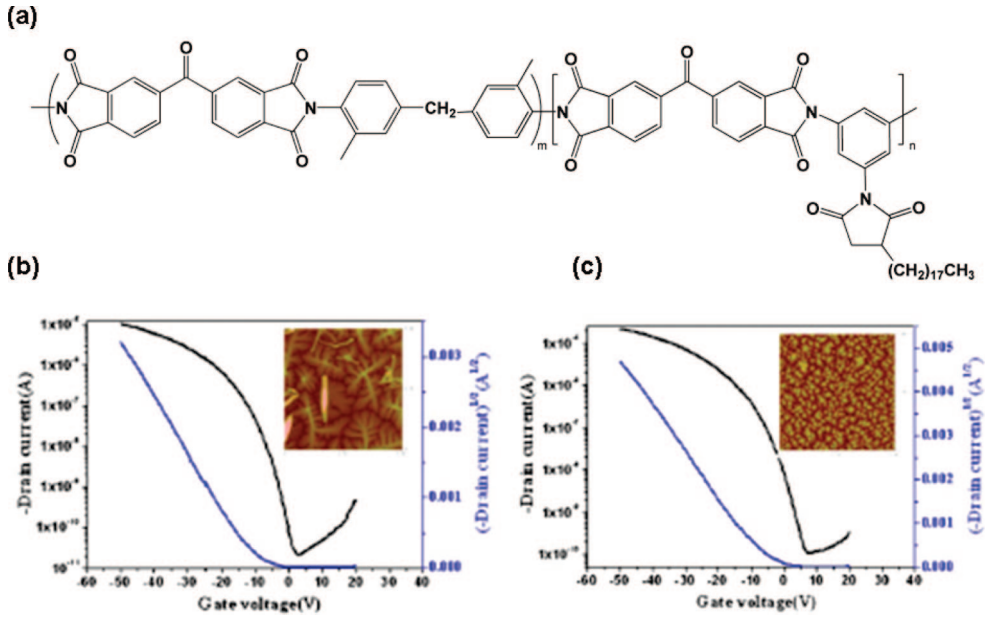


Figure 19. (a) Chemical structure of a low temperature processable, inherently photosensitive polyimide. (b) Transfer characteristics of a pentacene OFET with as-prepared polyimide on an ITO glass substrate. (c) Transfer characteristic curve of a pentacene OFET with the patterned polyimide on a PES substrate. The insets are AFM images (5 μm × 5 μm). Reprinted with permission from ref 143. Copyright 2005 American Institute of Physics.

FET component layers. Thus, SI-ROMP can compete with methods such as spin-coating, inkjet printing, and screen printing in the production of densely packed polymer layers.

In 2005, Pyo et al. reported a polyimide gate dielectric that fulfills some of the principal requirements for utility in low-cost fabrication processes: (i) they are patternable to easily access the gate electrode, and (ii) the processing temperature is rather low, in all cases below 150 °C.[143] The polyimide was prepared via a two-step reaction. First, the polyimide precursor, poly(amic acid), was prepared from a dianhydride and an aromatic diamine through a polycondensation reaction. Second, the precursor was converted to the corresponding polyimide by a chemical imidization. This polyimide layer exhibited good dielectric properties suitable for use as a gate dielectric in OFETs, with a leakage current below 5×10^{-8} A/cm^2 ($V = 0-100$ V), a breakdown voltage of 3 MV/cm, and a capacitance of 75 pF/mm^2. Previous reports on polyimide dielectrics indicated high leakage currents and high required processing temperatures.[126,144] Pyo et al. fabricated pentacene FETs both on ITO substrates with as-prepared polyimide dielectric layers and on polyethersulfone (PES) plastic substrates with photopatterned gate insulators. The electrical properties of both devices were similar, with $I_{ON}/I_{OFF} \approx 10^5$ and subthreshold slopes of ~3 V/dec. However, the field-effect carrier mobility was slightly lower for the patterned polyimide (0.1 cm^2 V^{-1} s^{-1}) than in the OFET with the as-prepared polyimide (0.2 cm^2 V^{-1} s^{-1}). The authors ascribed this to poor interface formation between the semiconductor and the gate dielectric caused by increased surface roughness (from 0.29 to 0.82 nm) and surface tension mismatch. Furthermore, a larger dendritic grain structure was observed for the pentacene film growth on the as-prepared polymide than on the photopatterned one, as shown by AFM images (see Figure 19).

Lim et al.[145] fabricated organic thin-film transistors on polyethersulfone (PES) using photocross-linkable PVP as the gate dielectric and pentacene as the organic semiconductor layer. They also analyzed the effects of the metal source/drain electrode work functions on the device performance, finding that the mobility abruptly increases as the work function increased up to 4.3 eV and, after that, increases only slowly. Using gold (5.34 eV) as the contact electrodes, they measured field-effect mobilities as high as 2.59 cm^2 V^{-1} s^{-1}.

A comparison between polymethylmethacrylate (PMMA) and PVP gate dielectrics was presented by Kang et al. using pentacene as the organic semiconductor and ITO as gate electrode.[146] The authors found better FET performance in the PVP-based device, with a field-effect mobility of 0.15 cm^2 V^{-1} s^{-1}, $V_T = 1.9$ V (0.045 cm^2 V^{-1} s^{-1} and −27.5 V for PMMA), while superior insulating properties were measured for the PMMA devices. The higher mobility of pentacene on PVP was attributed to larger grain sizes, hence more contiguous overlap of pentacene π-electron orbitals, while the large negative V_T for the PMMA transistors was ascribed to carrier trapping at grain boundaries and defects at the dielectric/semiconductor interface. The authors also analyzed the field and temperature dependence of the electrical properties. The PVP dielectric showed less field dependence, indicative of lower trap density. Temperature-dependent characterization of the PVP devices indicated that charge conduction is governed predominantly by hopping at high temperatures and predominantly by tunneling through the grain boundaries.

Yoon et al.[147] reported in 2005 on a method to decrease the polymer gate dielectric thickness by using cross-linked polymer blends (CPBs). The authors used two polymers (PVP and PS) and several cross-linking reagents (see Figure 20a). The cross-linking of the polymers (insolubility) ensures that subsequent layers can be spin-coated or printed on top without dissolution of the dielectric. These CPBs exhibit the largest k/d ratios and lowest leakage currents reported to date for such thin layers (10−20 nm) along with high capacitances (200−300 nF cm^{-2}). Moreover, they are pinhole-free. Optimum results were obtained for CPVP-C_6, and devices were fabricated using several p- and n-type organic semiconductors and different substrates, ranging from n+-Si, ITO-glass, ITO-Mylar, to kitchen aluminum foil, indicating good compatibility with all of them and very good stability

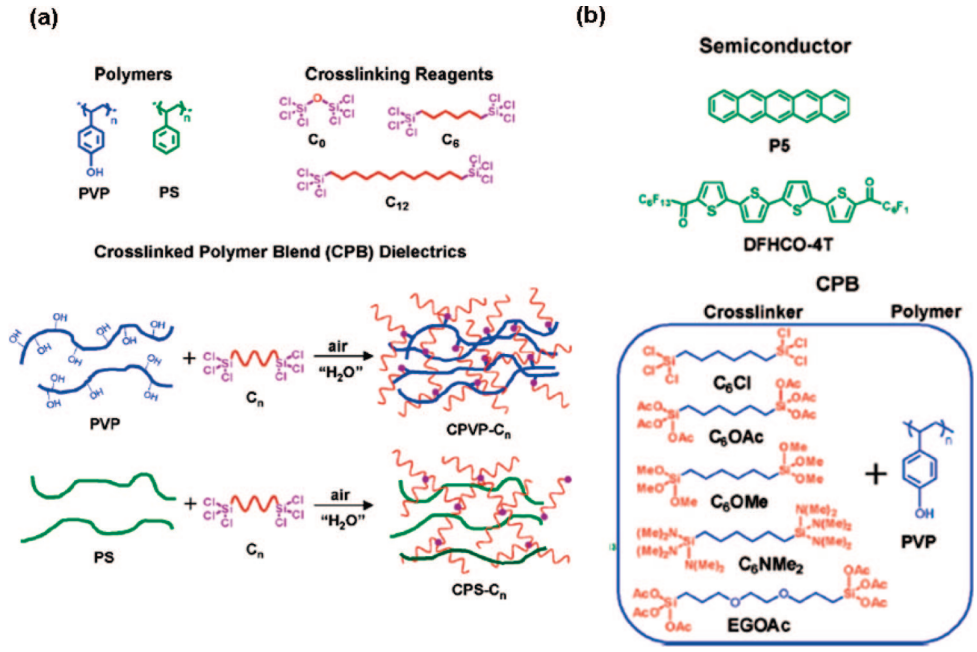


Figure 20. (a) Chemical structures of the polymers and cross-linkers employed in the CPB gate dielectric synthesis. Taken from ref 147. (b) Chemical structures of the organic semiconductors and of the CPB precursors employed to optimize the cross-linking and printing conditions. Reprinted with permission from ref 148. Copyright 2008 American Chemical Society.

to ambient atmosphere and bending. However, the surface morphologies are somewhat rough (rms roughness >2 nm) due to the high reactivity of the chlorosilane cross-linking reagents. In a more recent paper, these authors controlled and optimized the cross-linking conditions to minimize the roughness and to achieve printable solutions, by screening the reactivity of cross-linking chloro-, acetoxy-, dialkylamino-, and methoxy-silanes with PVP (Figure 20b).[148] For both ultrathin (<20 nm) and thick (50−500 nm) CPB films, they found that the moderately reactive EGOAc cross-linking reagent affords the smoothest film morphologies and superior dielectric response. They fabricated OFETs with both spin-coated and gravure-printed CPB films, recording mobilities of 0.12−0.49 and 0.02−0.52 $cm^2\ V^{-1}\ s^{-1}$ for pentacene and DFHCO-4T, respectively.

Han et al.[149] fabricated high-performance pentacene OFETs on PES using cross-linked PVP as the gate insulator and passivated pentacene films as organic semiconductor. To obtain patterned pentacene islands using a self-organizing process, oxygen plasma and OTS were applied to the PES surface to define hydrophilic and hydrophobic regions. The passivation layers on top of the semiconductor were 500 nm thick spin-coated polyvinylalcohol (PVA) and 1 μm thick photoacrylic layers. The OFETs, after the passivation step, exhibited a mobility of 0.80 $cm^2\ V^{-1}\ s^{-1}$, $V_T = -9.2$ V, and $I_{OFF}/I_{ON} = 10^8$. The authors analyzed the stability of these devices and reported a lifetime, defined as the time required to decrease the "on" current by one-half, of ~11 000 h in air. The mobility decreased with time for both passivated and unpassivated devices; however, threshold voltages increased for the unpassivated OFET, while they decreased for the passivated one. The authors ascribed the former effect to H_2O degradation and the latter effect to O_2 degradation.

Müllen et al.[150] used a soluble high-k poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) copolymer with an additional PMMA layer as the gate dielectric in P3HT devices. They measured a dielectric constant of about 11, which enables an increase in the transconductance and a reduction in the operational voltages of the corresponding devices. Using layers of 2 μm thickness, the resulting transistors were free of hysteresis, making them suitable for operation as logic elements. Reduction of the dielectric thickness, below 1 μm, induced ferroelectric hysteresis in the copolymer, that Müllen et al. argued could be interesting for application as memory elements. Lee et al.[151] prepared photopatternable PVP (P-PVP) and applied it to fabricating high performance pentacene OFETs on plastic, with a field-effect mobility of 1.23 $cm^2\ V^{-1}\ s^{-1}$, $V_T = -6.5$ V, and $I_{ON}/I_{OFF} = 10^7$. The P-PVP dielectric layer was obtained from a PVP precursor solution composed of PVP (74 wt %), 1,2,4,5-tetraacetoxymethylbenzene (16 wt %, cross-linking material), and 2,4-bis(trichloromethyl)-6-aryl-1,3,5-triazine (10 wt %, photoacid generator). This PVP solution was spin-coated, and the resulting films were patterned using conventional photolithography; they exhibited a leakage current below 0.01 $\mu A/cm^2$ at 1 MV/cm.

Diallo et al.[152] studied the stability of pentacene top-gate devices using poly-p-xylylene (parylene) as the dielectric material. The substrate was a 125 μm thick Kapton foil covered with a planarization polymer layer. Interdigited source/drain contacts were first evaporated through a shadow mask, followed by a 70 nm thick pentacene layer. The gate dielectric was a 540 nm thick parylene-C layer with a dielectric constant of $k = 3.1$, and the top-gate electrode was 100 nm thick evaporated Al. The devices were characterized in the dark and under two different atmospheres (vacuum and air), affording similar results. Indeed, most of the transport parameters were not significantly affected by the ambient ($I_{ON}/I_{OFF} > 10^4$, $S = 2$ V/dec, $V_T = -3.5$ V). However, the subthreshold current increased by almost 2 orders of magnitude when the device was characterized in air. The authors related this fact to the creation of interface states. They also analyzed the stability of the devices after bias stress, finding that the electrical parameters were not affected by applying stress at positive gate voltage $V_G = +20$ V for 70 min. After 70 min of bias stress, a small positive shift of the onset voltage was seen; however, the mobility was not altered.

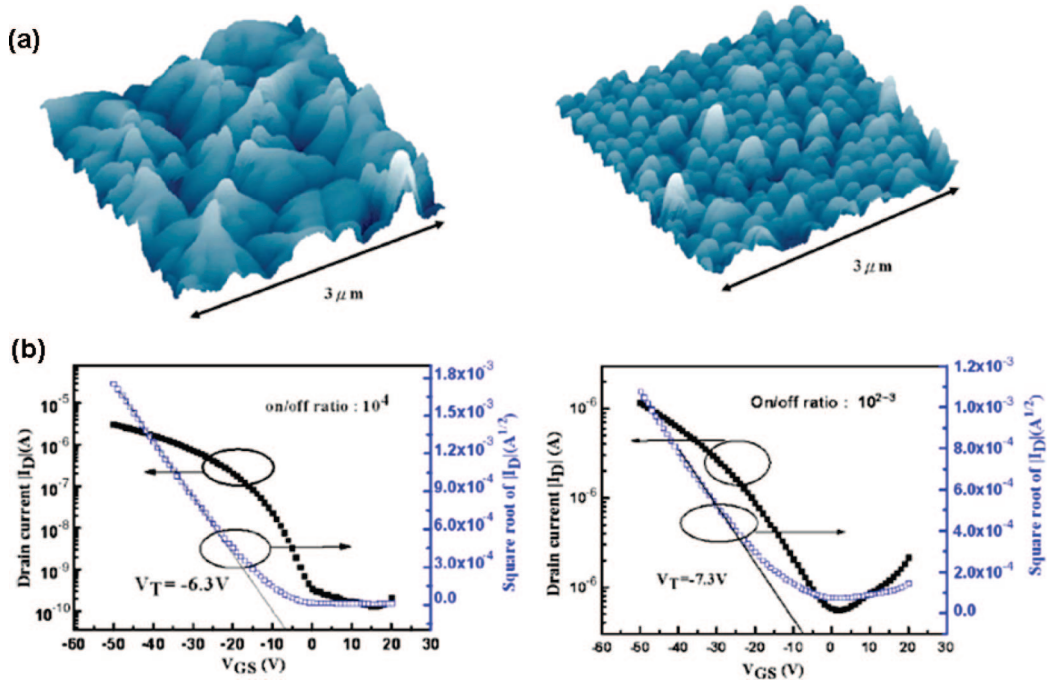


Figure 21. (a) AFM images of pentacene films grown on PMMA (left) and SiO_2 (right) dielectrics. (b) Transfer characteristics of a pentacene OFET with PMMA (left) and SiO_2 (right) as the gate dielectric layer. Reprinted with permission from ref 153. Copyright 2007 American Institute of Physics.

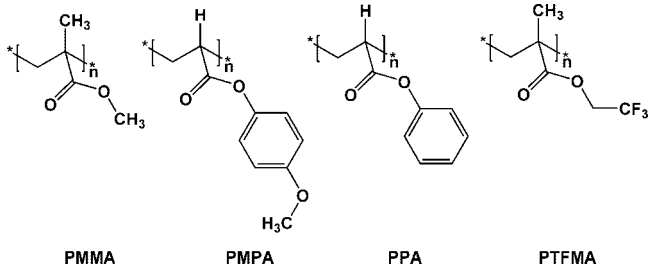


Figure 22. Chemical structures of dielectric polymers PMMA, PMPA, PPA, and PTFMA.

Huang et al.[153] investigated the properties of pentacene-based OFETs using polymethylmethacrylate (PMMA) as the gate dielectric and compared them to thermally grown SiO_2. The authors observed larger pentacene grain sizes (1000−1500 nm on PMMA vs 100−300 nm in SiO_2) and a better crystalline quality of the pentacene thin films on PMMA as compared to SiO_2, which translated to superior electrical performance (see Figure 21a). Furthermore, the near-perfect matching of the surface free energy of pentacene with PMMA (47.4 mJ m^{-2}/47.5 mJ m^{-2}) yielded a field-effect mobility of 0.241 $cm^2\ V^{-1}\ s^{-1}$, $V_T = -6.3$, and $I_{ON}/I_{OFF} \approx 10^4$ versus $\mu = 0.0372\ cm^2\ V^{-1}\ s^{-1}$, $V_T = -7.3$, and $I_{ON}/I_{OFF} \approx 10^3$ for SiO_2 (see Figure 21b).

Recently, Cheng et al.[154] analyzed the effect of dielectric chemical structure by evaporating pentacene onto a series of polyacrylates having different functionalizations: poly(methylmethacrylate) (PMMA, $k = 3.2$), poly(4-methoxyphenylacrylate) (PMPA, $k = 3.4$), poly(phenylacrylate) (PPA, $k = 2.9$), and poly(2,2,2-trifluoroethyl methacrylate) (PTFMA, $k = 6.0$) (see chemical structures in Figure 22). AFM experiments indicated that PMMA, PMPA, and PPA induce layer-by-layer pentacene growth, while PTFMA induces island growth, where smaller grain sizes are typically found. Nonetheless, the latter films on PTFMA exhibit the largest mobility, 0.195 $cm^2\ V^{-1}\ s^{-1}$, which was ascribed to the growth of pentacene single crystals. The authors also found

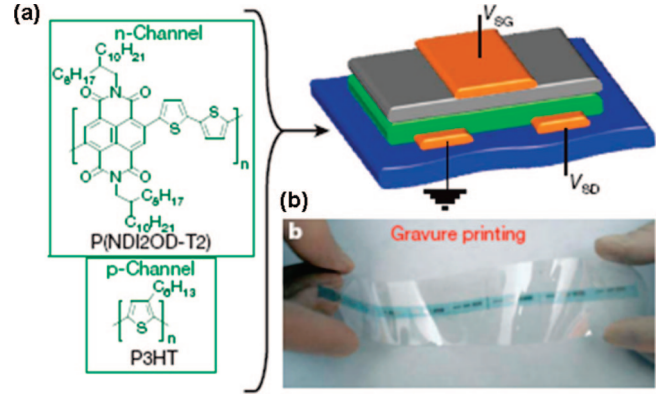


Figure 23. (a) Chemical structures of P(NDI2OD-T2) and P3HT, and illustration of the top-gate bottom-contact FET architecture used in this study. (b) Optical images of gravure-printed top-gate bottom contact FETs on PET before top-gate contact deposition. Reprinted with permission from ref 52. Copyright 2009 Macmillan Publishers Ltd.

a dependence of the charge-carrier mobility on the dipole moment of the dielectric side-chain terminal groups. They also demonstrated that threshold voltage in these devices could be easily controlled by tuning the polymer dielectric.

In 2009, Yan et al.[52] fabricated high-mobility electron-transporting printed OFETs using a family of dielectric materials encompassing a variety of chemical structures, surface energies, and dielectric constants. The polymeric insulators used were a poly(perfluoroalkenylvinyl ether) (CYTOP, $k = 2.0$), poly(*t*-butylstyrene) (PTBS, $k = 2.4$), polystyrene (PS, $k = 2.5$), a polyolefin-polyacrylate (ActivInk D2200, $k = 3.2$), and poly(methylmethacrylate) (PMMA, $k = 3.6$). The transistors were fabricated using poly{[*N*,*N*′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)2,6-diyl]-*alt*-5,5′-(2,2′-bithiophene)} (P(NDI2OD-T2) as the n-type semiconductor (see Figure 23), and they exhibited mobilities ranging from 0.45 to 0.85 $cm^2\ V^{-1}\ s^{-1}$ depending on the substrate, dielectric, and deposition method used. The

Table 2. Summary of the Dielectric and OFET Characteristics for Various Polymeric Gate Dielectrics

ref	dielectric	method[a]	D (nm)	C_i (nF cm^{-2})	k	E_B (MV/cm)	semiconductor	μ (cm^2 V^{-1} s^{-1})	I_{ON}/I_{OFF}	year
123	CYEPL	cast		6	18.5		6T	0.034		1990
	PVA			10	7.8			0.00093		
124	CYEPL	cast			18.5		6T	0.43		1990
125	polyester		1500		3		DH-6T	0.06		1994
126	polyimide	print		20			poly(3-hexylthiophene)	0.01−0.03		1997
129	PVP	SC	400−500				F8T2	0.01−0.02	10^{+5}	2000
130	polyimide	cast	2000	1			6T	0.01		2000
							F16CuPc	0.001		
133	GR	SC	>1000	0.43−4.97			6T	∼0.006	$\sim10^{+2}$	2002
							DH-5T	∼0.04	$10^{+2}-10^{+3}$	
							PcCu	∼0.003	$\sim10^{+2}$	
							pentacene	∼0.1	$10^{+3}-10^{+5}$	
136	PVP	SC	440		4.2		pentacene	0.1	10^{+3}	2002
							poly(3-hexylthiophene)	0.002	10^{+2}	
137	cross-linked PVP	SC	260		3.6		pentacene	3	10^{+5}	2002
	PVP copolymer	SC	380		4		pentacene	2.9	10^{+5}	
139	CYPEL	SC	1200	8.85	12		poly(3-butylthiophene)	0.04		2004
	PVP		900	5.59	5			0.0002		
	PVA		500	17.8	10			0.03−0.003		
140	PVAc/PVP	SC	1000 (PVAc) + 20 (PVP)				pentacene	0.1	10^{+5}	2004
37	BCB	SC	50	235		>3	poly(9,9-dialkylfluorene-*alt*-triarylamine)	∼10−4		2004
142	polynorbornene	SI-ROMP	∼1200	∼3			pentacene	0.1−0.3	$\sim10^{+2}$	2004
143	polyimide	reaction		7.5		3	pentacene	0.1−0.2		2005
145	photocross-linkable PVP	SC	600				pentacene	2.59		2005
147	CPVP-Cn	SC	∼15	∼300	∼6	3−6	pentacene	0.1	$\sim10^{+4}$	2005
	CPS-Cn		∼15	200−220	∼3	3−6		0.08	$\sim10^{+4}$	
149	cross-linked PVP	SC	450				pentacene	0.8	10^{+8}	2006
150	P(VDF-TrFE)+ PMMA	SC	2000		∼11		poly(3-hexylthiophene)			2006
151	photopatternable PVP	SC					pentacene	1.23	10^{+7}	2007
152	parylene-C		540		3.1		pentacene		$>10^{+4}$	2007
153	PMMA	SC	300				pentacene	0.241	$\sim10^{+4}$	2007
148	CPB (PVP)	SC	305	18		3−6	pentacene	0.49	10^{+7}	2008
							DFH-CO-4T	0.52	10^{+5}	
		GP	450−550	5.5−7.5			pentacene	0.29−0.85	$10^{+4}-10^{+6}$	
							DFH-CO-4T	0.38−0.86	$10^{+5}-10^{+6}$	
154	PMMA	SC	560	5.06	3.2		pentacene	0.153	$\sim10^{+4}$	2008
	PMPA		660	4.56	3.4			0.134	$\sim10^{+4}$	
	PPA		582	4.41	2.9			0.093	$\sim10^{+4}$	
	PTFMA		592	5.35	6			0.195	$\sim10^{+4}$	
52	CYTOP	SC	450−600		2		P(NDI2OD-T2)	0.1−0.25	$10^{+6}-10^{+7}$	2009
	PTBS		600−800		2.4			0.1−0.4	$10^{+6}-10^{+7}$	
	PS		500−700		2.5			0.1−0.3	$10^{+7}-10^{+8}$	
	ActivInk D2200		350−500		3.2			0.2−0.85	$10^{+6}-10^{+7}$	
	PMMA		600−900		3.6			0.2−0.45	$10^{+6}-10^{+7}$	

[a] Dielectric deposition method. Abbreviations: SC, spin coating; SIROMP, surface-initiated ring-opening metathesis polymerization; GA, gravure printing.

authors found little sensitivity of the mobility to the dielectric constant of the insulator, which indicated very efficient electron transport within the polymeric semiconductor. Furthermore, the n-type polymer presented in this work was used in the fabrication of the first spin-coated and gravure-printed polymeric semiconductor complementary inverters (using P3HT as the p-type material; see Figure 23) operating in ambient conditions.

Table 2 summarizes dielectric and OFET characteristics for various polymeric gate dielectrics.

3.2.2. Self-Assembled Mono- and Multilayers

One class of organic gate dielectrics that has received great interest is self-assembled monolayers (SAMs) and self-assembled multilayers (SAMTs). In these cases, the principal strategy has been to increase the capacitance of the dielectric by decreasing the thickness of the organic layer to a few nanometers without incurring leakage currents. Layers of SiO_2 in this thickness range exhibit very poor insulating behavior, with leakage currents as high as $10^{-3}-10^{-1}$ A/cm^2. In contrast, leakage currents on the order of $\sim10^{-8}$ A/cm^2 are found for some SAMs and SAMTs. However, and despite its importance, in this contribution we will not exhaustively analyze this area of dielectrics because there exist several other reviews that focus on advances in this field.[36g,155] Thus, only a brief summary will be presented here. The use of a SAM as a gate dielectric was pioneered by Vuillaume in 1996 by the deposition of octadecyltrichlorosilane (OTS) onto the native oxide of Si wafers, yielding leakage currents of $\sim10^{-8}$ A/cm^2 (see chemical structure in Figure 24a).[156] In later contributions, this group also investigated: (i) the effect of varying the SAM alkyl chain length, and they claimed that leakage could be avoided by controlling the layer organization and packing density of the organic layer even though the SAMs were only ∼2 nm thick, and with a conductivity similar to that of the bulk material,[157] and (ii) the effect of various SAM functionalizations. In particular, they studied three different alkyltrichlorosilanes end groups ($-CH_3$, $-CH{=}CH_2$, $-COOH$), all exhibiting leakage current densities below $10^{-5}-10^{-8}$ A/cm^2.[158] Vuillaume et al.

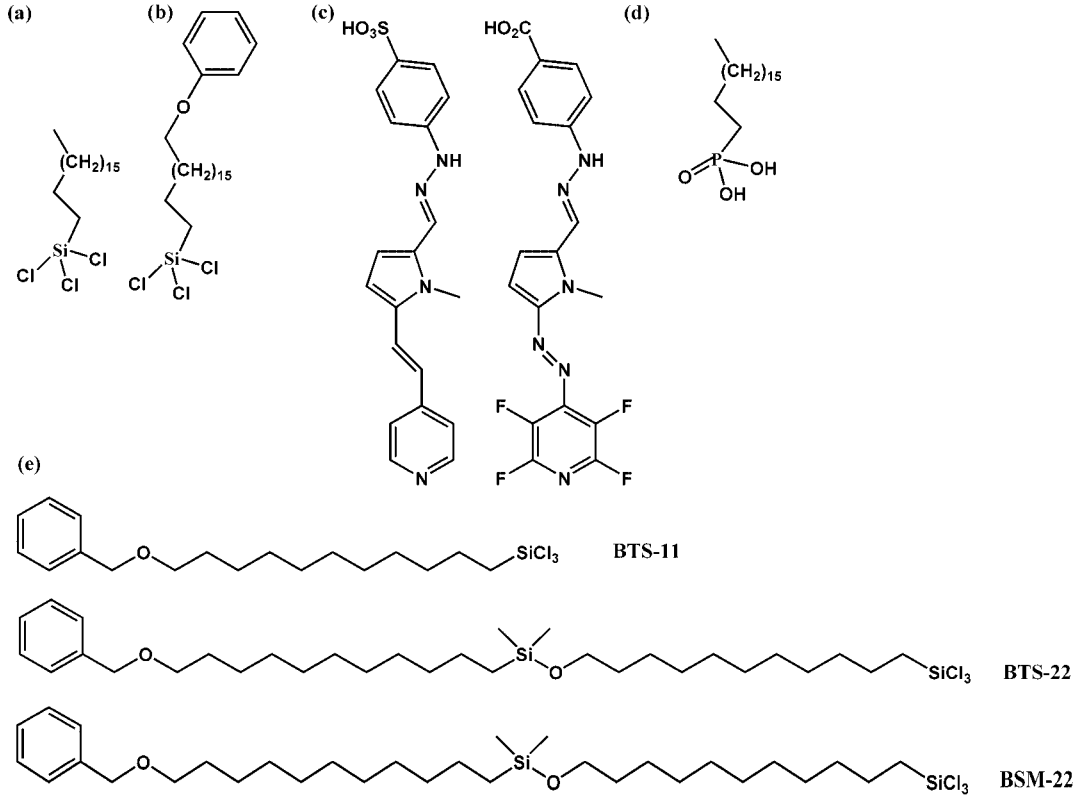


Figure 24. Chemical structures of self-assembled monolayer precursors used as gate dielectrics in OFETs.

demonstrated that the use of a SAM having a −COOH end group as the gate insulator in a 6T-based OFET achieved respectable performance ($\mu \approx 10^{-4}$ cm^2 V^{-1} s^{-1}, $I_{ON}/I_{OFF} = 10^4$, and $V_T = -1.3$ V).[158b] Halik et al. also reported the suitability of OTS monolayers as gate dielectrics in OFETs using alkyl-substituted oligothiophenes as the organic semiconductors. They reported that long side chains increase the effective thickness of the gate dielectric, reducing the gate currents and achieving mobilities as large as 0.05 cm^2 V^{-1} s^{-1} for the hexyl-substituted sexithiophene.[159] Later, using phenoxy-terminated alkyltrichlorosilanes, they deposited closely packed monolayers having arene−arene $\pi-\pi$ interactions that are thought to avoid penetration of the SAM by the semiconductor molecules (see Figure 24b). The leakage currents were reported to be $\sim 10^{-8}$ A cm^{-2} at a voltage of 1 V. Pentacene-based devices were fabricated and exhibited a field-effect mobility of 1 cm^2 V^{-1} s^{-1}, $I_{ON}/I_{OFF} \approx 10^6$, and $V_T \approx -1.3$ V.[39]

In the past several years, the Northwestern University group has investigated a special type of self-assembled nanodielectric (SAND) grown by depositing alternating σ (Alk) and π (Stb) constituent molecular layers, and having an octachlorotrisiloxane-derived capping layer to stabilize/planarize the assembly and to regenerate a reactive hydroxyl surface for subsequent monolayer deposition.[40] Depending on the constituent molecules used, type-I, type-II, and type-III SANDs were fabricated with maximum capacitances $C = 400$ (type-I), 710 (type-II), and 390 (type-III) nF cm^{-2} at 10^2 Hz (see Figure 25). Both p-type and n-type OFETs were fabricated with SANDs as gate dielectrics, affording mobilities comparable to OFETs obtained with SiO_2 dielectrics but at far lower operating voltages. The compatibility of type-III SANDs (III-3, with 3 repeating SAND trilayers, $d = 16.5$ nm, $C = 180$ nF cm^{-2}) with inorganic semiconductors was also demonstrated with 60 nm thick In_2O_3 in fully transparent devices.[160] Mobilities as high as 120−140 cm^2 V^{-1} s^{-1} were reported. In addition, type III-3 SAND was also demonstrated to enhance the power consumption efficiency of ZnO nanowire-based OFETs ($\mu = 196$ cm^2 V^{-1} s^{-1}), to be compatible with photolithography and e-beam evaporation methodologies, and to be chemically and thermally robust, as well as radiation-hard.[161] In a subsequent paper, the excellent SAND compatibility with single-wall carbon nanotube (SWCNT) semiconductors was also reported.[162] In this work, SWCNTs were grown by CVD onto Si/SiO_2 substrates and then printed directly onto the III-3 SAND dielectric. Figures of merits of $\mu \approx 5.6$ cm^2 V^{-1} s^{-1} and $V_T = 0.2$ V were achieved with greatly reduced hysteresis. SWCNT-based high-performance FETs were later demonstrated by Klauk et al. using (18-phenoxyoctadecyl)-trichlorosilane as gate dielectric (Figure 24b).[74e] Finally, the III-3 SAND dielectric was also demonstrated to be compatible with solution-processed cadmium selenide (CdSe) semiconductor layers, which require thermal annealing at 400 °C.[163] The field-effect mobilities reported for CdSe were as high as 57 cm^2 V^{-1} s^{-1} with large I_{ON}/I_{OFF} ratios (10^5) and subthreshold slopes as low as 0.26 V dec^{-1}.

In efforts to further optimize SAND properties, two strategies were pursued simultaneously by the Northwestern group: (i) incorporation of higher-k molecules (see chemical structures in Figure 24c), and (ii) use of a room-temperature vapor phase deposition procedures (v-SANDs).[164] Pentacene OFETs fabricated with these v-SANDs exhibited very large mobilities of 2−3 cm^2 V^{-1} s^{-1} and $I_{ON}/I_{OFF} \approx 10^5$, demonstrating a clear enhancement as compared to the solution-based SANDs. Following this same research line, improved electrical performance was also claimed by Zuppiroli et al. using vapor-deposited anthracene-9-carboxy acid and phenylundecanoid acid monolayers.[165]

Klauk et al.[75d] reported the first growth of n-octadecylphosphonic acid (ODPA) monolayers (Figure 24d) on evaporated, patterned aluminum gates, using glass substrates.

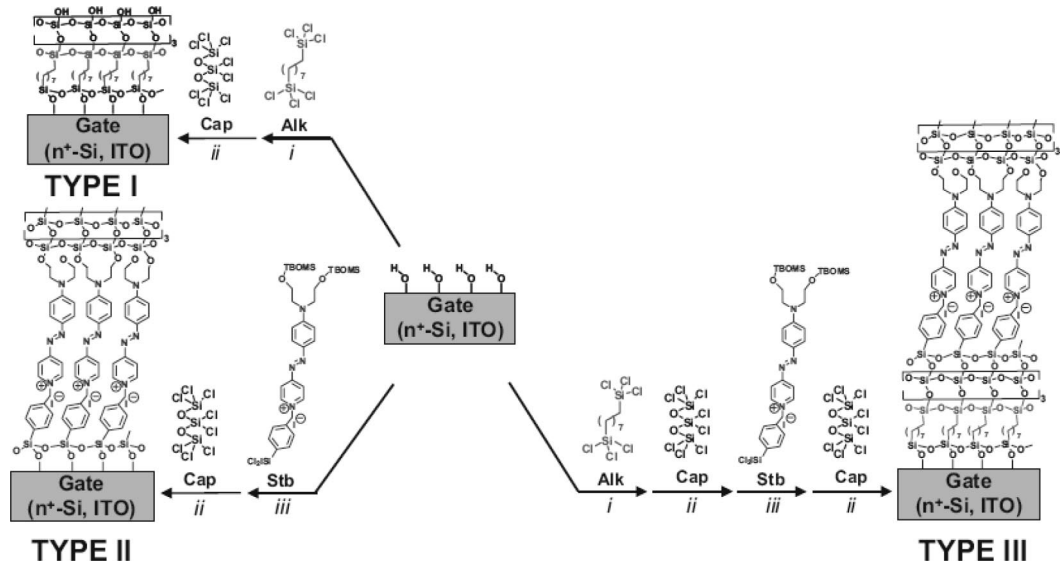


Figure 25. Schematic depiction of the fabrication of SANDs (self-assembled nanodielectrics) types I, II, and III. Reprinted with permission from ref 36g. Copyright 2005 Wiley−VCH Verlag GmbH & Co. KGaA.

Leakage currents of $\sim 10^{-8}$ A cm^{-2} were reported at an applied voltage of 2 V, and a capacitance of 0.7 μF cm^{-2} was also reported. Both p-type pentacene and n-type F_{16}CuPc semiconductors were tested using ODPA as the gate dielectric, obtaining mobilities of 0.6 and 0.02 cm^2 V^{-1} s^{-1}, respectively. In addition, complementary circuits and ring oscillators were fabricated with a static power consumption of less than 1 nW per logic gate. In a subsequent report, these authors went a step further and used microcontact-printed ODPA monolayers, first as an etch resist to pattern the aluminum gate electrodes by wet etching, and then as the gate dielectric in the same devices.[75e] They again fabricated pentacene and F_{16}CuPc based-OFETs and found mobilities similar to those discussed above.[75d]

Recently, Kim et al.[89] investigated organic monolayers of (benzyloxy)alkyltrichlorosilane (BTS) (see chemical structure in Figure 24e) with varying chain lengths (BTS-11 and BTS-22), and of a (benzyloxy)alkyltrimethoxysilane (BSM-22), both on 2 nm thick SiO_2 (NO_X) and on a thin layer of oxygen plasma grown Al_2O_3 (MTO_X). Pentacene devices were then fabricated with these dielectric monolayers. Kim et al. found that longer alkyl chain, NO_X/BTS-22, afforded sufficiently low gate leakage currents to produce transistors with relatively good performance parameters ($\mu \approx 0.12$ cm^2 V^{-1} s^{-1}, $I_{ON}/I_{OFF} \approx 10^2$, and $V_T \approx -0.50$ V). In contrast, shorter alkyl chains, NO_X/BTS-11, exhibited moderately large leakage currents and displayed inferior OFET performance characteristics. BSM-22 and BTS-22 monolayers on MTO_X exhibited degraded transistor performance, probably due to damage of the Al_2O_3 surface during the self-assembly procedure.

3.3. Hybrid Dielectrics

So far, two principal strategies to increase capacitance and hence, transistor characteristics, have been reviewed: (i) utilization of high-k inorganic materials and (ii) utilization of easily processable organic dielectrics. Both strategies offer advantages and disadvantages. In particular, even if high-k metal oxides are ideal candidates for fabricating high-capacitance OFETs capable of low-voltage operation, most of them are based on ceramics, which require generally expensive deposition equipment and usually require high-temperature annealing processes, both incompatible with plastic substrates. Furthermore, the generally poor mechanical properties of these materials render them challenging to use in flexible electronics. On the other hand, easily processable polymers typically have low dielectric constants and good mechanical properties, but require large gate dielectric thicknesses due to high leakage currents. A new approach is to combine inorganic−organic materials as gate dielectrics. These complementary constituents ideally combine high permittivity of the inorganic inclusions and high breakdown strength, mechanical flexibility, and easy processability of the organic counterparts. In this Review, we focus on three types of hybrid inorganic−organic dielectrics: polymeric−nanoparticle composites, inorganic−organic bilayers, and hybrid solid polymer electrolytes (see Tables 3 and 4).

3.3.1. Polymeric−Nanoparticle Composites

One of the first reports studying polymer−nanoparticle insulators appeared in 1988 and focused on TiO_2 nanoparticle−polystyrene (PS) composites as dielectric materials. Nevertheless, this first attempt resulted in an inhomogeneous system with problems of porosity (air pockets) in the composite material.[166] In 2004, Chen et al. prepared nanocomposite dielectric layers using cross-linked poly-4-vinylphenol (PVP) and TiO_2 nanoparticles ($k = 80$), which could be deposited by spin-coating.[167] Different formulations of this dielectric were tested, principally by changing the nanoparticle concentrations. They then fabricated vapor-deposited pentacene-based OFETs using patterned ITO on a glass substrate as the gate electrode and found that an additional PEDOT (30 nm) layer on the ITO enhanced the I_{ON}/I_{OFF} from 10^3 to 10^4. After inserting the additional layer, the dielectric constant increased from 3.5 for pure cross-linked PVP to 3.9, and it reached 5.4 for the dielectric film with 7 wt % of TiO_2 nanoparticles, the highest nanoparticle concentration prepared. Chen et al. found that pentacene devices with 7 wt % TiO_2 nanoparticles/PVP as the gate insulator yield almost twice the field-induced current at the same gate voltage and increase the field-effect mobility from 0.20 to 0.24 cm^2 V^{-1} s^{-1}. However, one of the difficulties that these nanocomposites present is increased leakage current as compared to pure, cross-linked PVP, translating

Table 3. Summary of the Dielectric and OFET Characteristics of Various Polymer−Nanoparticle Composite Gate Dielectrics

ref	dielectric (nanocomposites)[a]	method[b]	D (nm)	loading (%)	C_i (nF cm^{-2})	k	E_B (MV/cm)	semiconductor	μ (cm^2 V^{-1} s^{-1})	I_{ON}/I_{OFF}	year
167	cross-linked PPV + TiO_2	SC	700	7 (wt)		5.4		pentacene	0.24	10^{+3}	2004
168	PS-TiO_2	SC	500−1200	18.2 (vol)		9.4−8		pentacene	0.2	535	2005
184	$BaTiO_3$ + PVAIA	SC	170		62.5	12		pentacene	0.12	$\sim 5 \times 10^{-3}$	2005
	$BaTiO_3$ + PVAIA	SC				9		pentacene	0.4		2005
	$BaTiO_3$ + PVA	SC	160		61	10.9		pentacene	0.35	$\sim 10^{+4}$	2005
169	PS-TiO_2	SC				8.2		pentacene	1.3	$\sim 10^{+3}$	2007
171	polypropylene + $BaTiO_3$	DB					4				2007
	polypropylene + TiO_2	DB					4				2007
173	TiO_2 + Nylon-6	SC	∼350			14		pentacene	0.1	$\sim 10^{+3}$	2007
	TiO_2 + Nylon-6 + PVP (t.)	SC	∼350 + 30 (PVP)			11		pentacene	0.7	$\sim 10^{+4}$	2007
174	SM-$BaTiO_3$ + PVP	SC	406	37 (vol)	31	14		pentacene	0.04	6×10^4	2008
	SM-$BaTiO_3$ + PVP + PVP (t.)	SC		37 (vol)	42	12		pentacene	0.17	$\sim 10^{+5}$	2008
175	SM-TiO_2 + polyimide	SC	400−500	2 (vol)		∼4		pentacene	∼0.18	6×10^5	2008
185	SM-Al_2O_3 + PVP	SC	290	24 (vol)		7.2		pentacene	∼0.25	$\sim 10^{+3}$	2008

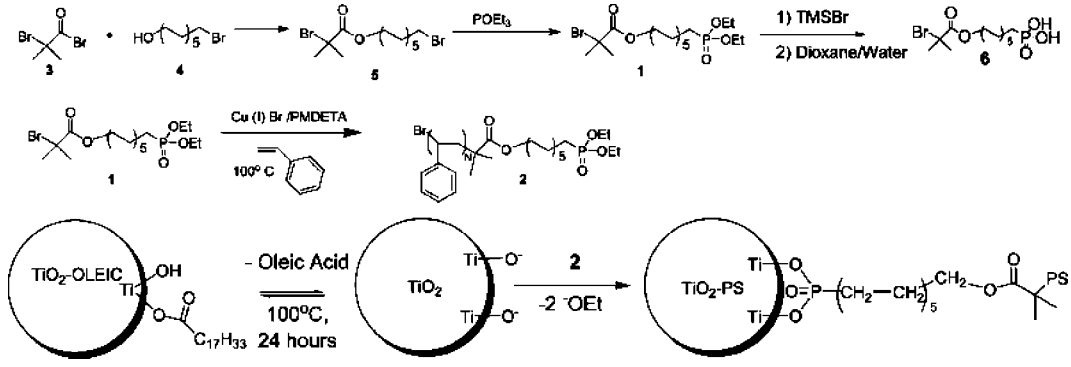
[a] t indicates a thin film of the corresponding polymer. SM stands for surface modified. [b] Dielectric deposition method. Abbreviations: SC, spin coating; DB, doctor blading.

Table 4. Summary of the Dielectric and OFET Characteristics of Various Inorganic−Organic Bilayer Gate Dielectrics

ref	dielectric (bilayer)	method[a]	D (nm)	C_i (nF cm^{-2})	E_B (MV/cm)	semiconductor	μ (cm^2 V^{-1} s^{-1})	I_{ON}/I_{OFF}	year
189	Ta_2O_5/PMMA	e-beam/SC	120 (Ta_2O_5) + 37 (PMMA)	39		pentacene	0.3	$\sim 10^5$	2005
104	TiO_2/PAMS	anodiz./SC	7.5 (TiO2)/10 (PAMS)	228		pentacene	0.8		2005
105	TiO_2/OTS	anodiz./SC		465		pentacene	0.25	10^3-10^4	2005
190	Al_2O_3/PMMA	anodiz./SC	100 (Al_2O_3) + 160 (PMMA)	11.6		pentacene	∼0.3		2006
191	HfO_2/epoxy	ALD/SC		∼330		SWCNT	∼13	$\sim 10^3$	2006
192	SiO_2/cross-linked PVA	PECVD/SC	950 (PVA) + 350 (SiO_2)			pentacene	0.12	$\sim 10^6$	2006
193	YO_x/PVP	e-beam/SC	100 (YO_x) + 45 (PVP)	47.1	2	pentacene	0.83	$\sim 10^4$	2006
	YO_x/PVP	e-beam/SC	100 (YO_x) + 70 (PVP)	35.2	2	pentacene	0.4	$\sim 10^4$	
194	Ta_2O_5/cross-linked PVP	anodiz./SC	120 (Ta_2O_5) + 250 (PVP)	11.6		P3HT	0.03		2007
64b	Ta_2O_5/cross-linked PVP	sputt./SC	100 (Ta_2O_5) + 50 (PVP)			pentacene	0.46−0.48		2007
101	Ta_2O_5/PMMA	e-beam/SC	80 (Ta_2O_5) + 37 (PMMA)	63.5		pentacene	0.68	$\sim 10^5$	2008
196	PVP/HfO_2/PVP	SC/ALD/SC	200 (PVP) + 10 (HfO_2) + 200 (PVP)			pentacene	0.56	$\sim 10^6$	2008
197	HfO_2/SAM	sol−gel	3.1 (HfO_2)	580−690		pentacene	0.15−0.33	$\sim 10^5-10^6$	2008
198	HfO_2/ODPA	sol−gel	3.1 (HfO_2)	560		C_{60}	0.28	$\sim 10^5$	2008
199	Al_2O_3/cross-linked BCB	ALD/SC	100 (Al_2O_3)	50	>3	C_{60}	∼2.5	$\sim 10^6$	2008

[a] Dielectric deposition method. Abbreviations: SC, spin coating; anodiz., anodization; ALD, atomic layer deposition; PECVD, plasma-enhanced chemical vapor deposition.

Scheme 1. Synthesis of Phosphonate-Terminated Polystyrene (2) and Ligand Exchange Reaction of Diethyl-Phosphonate-Terminated Polystyrene 2 with Oleic Acid-Terminated TiO_2 Nanoparticles To Generate Polystyrene-Coated TiO_2 Nanoparticles (TiO_2-PS) (PMDETA = Pentamethyldiethylenetriamine)[a]

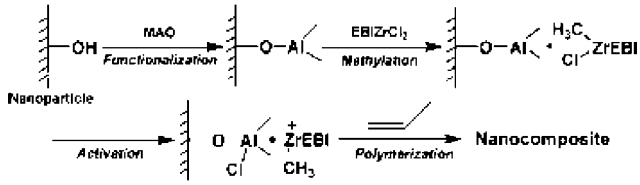


[a] Reprinted with permission from ref 168. Copyright 2005 American Chemical Society.

to a decreased I_{ON}/I_{OFF} by an order of magnitude. Furthermore, the device performance is still limited by the solubility/dispersibility of the TiO_2 nanoparticles in solution, leading to nanoparticle agglomeration at higher concentrations.

In 2005, Maliakal et al.[168] fabricated TiO_2−PS polymer shell nanocomposites via a ligand exchange reaction between oleic acid-stabilized titanium oxide nanoparticles (TiO_2−OLEIC) and diethyl phosphonate terminated polystyrene, leading to effective dispersion and enhanced dielectric properties as compared to previous results (see Scheme 1). Thus, TiO_2−OLEIC nanoparticles (anastase phase) are cylindrical in shape and disperse well in chlorobenzene. Capacitors were next fabricated by spin-coating TiO_2−PS (18.2% volume TiO_2) suspensions from chlorobenzene solution onto ITO on glass, yielding films of thicknesses ranging from 0.5 to 1.25 μm, and exhibiting up to a 3.6 times enhancement in k versus PS. Pentacene-based TFT devices were then fabricated, and they exhibited mobilities of 0.2 cm^2 V^{-1} s^{-1} and low threshold voltage of −2 V, indicating a low trap density and dielectric compatibility with pentacene

Scheme 2. Synthesis of Isotactic Polypropylene−Metal Oxide Nanocomposites[a]



[a] Reprinted with permission from ref 171. Copyright 2007 American Chemical Society.

film growth and good adhesion. Dielectric breakdown occurs at fields exceeding 2×10^6 V/m. In a following paper, the authors analyzed the blending of the aforementioned TiO_2−PS nanocomposites[168] into PS thin films to investigate permittivity effects on OFET performance over a broad range of permittivities (2.5−8.0) while keeping the surface energy essentially constant.[169] Maliakal et al. found that the dielectric constant of these blends increases roughly linearly with the TiO_2−PS nanocomposite loading, and, consequently, the mobility of pentacene transistors also increases from 0.015 to 1.3 $cm^2\ V^{-1}\ s^{-1}$, with the latter being the highest value recorded for 100% TiO_2−PS, without PS blending. This value is much larger than that previously reported[168] due to optimization of the solvent evaporation conditions. Furthermore, the significant enhancement in mobility with high-k TiO_2−PS is ascribed here to morphological changes, suggesting that the high mobility of pentacene on TiO_2−PS might be due to more efficient charge transfer between better connected small grains, in contrast to previous studies[170] where high mobility was correlated with large crystalline domains in the pentacene layers.

In 2007, Marks et al.[171] reported a method to disrupt nanoparticle agglomeration via in situ polymerization using metallocene catalysts supported on ferroelectric oxide nanoparticles. By coating the nanoparticles with methylalumoxane (MAO), followed by in situ propylene polymerization, they obtained homogeneously dispersed $BaTiO_3$ and TiO_2 nanoparticles within the matrix of a processable, high-strength polypropylene (see Scheme 2). These conclusions were supported by TEM and SEM experiments; TEM images show the homogeneous dispersion of the nanoparticles in the polypropylene matrices, while SEM images were consistent with polymer chain growth from the nanoparticles (Figure 26). The excellent quality of the insulators was evidenced by low leakage current ($\sim 10^{-6}$ to 10^{-9} A/cm^2 at 200 V) and high breakdown strengths (~4 MV/cm), consistent with homogeneous inclusion of the metal oxide nanoparticles.

In the same year, Lee et al.,[172] also seeking improved dispersion stability of TiO_2 nanoparticles, added surfactants (polysorbate 80, Tween80) to the solution mixtures and studied the dispersion, measuring the sedimentation time of TiO_2 particles in a PVP solution. As expected, the surfactant aids TiO_2 dispersion in the polymer matrix; however, some aggregation was still found that increased leakage currents and eroded the device performance as compared to the pure polymer. Another strategy to reduce the leakage current was proposed by Kim et al.[173] In their work, a solution-processed high dielectric gate insulator was fabricated by dispersing high-k TiO_2 nanoparticles in a Nylon-6 polymer matrix. However, it was found that even if the nanoparticles were uniformly dispersed in the polymer matrix, an additional PVP polymer buffer layer was necessary to suppress the leakage

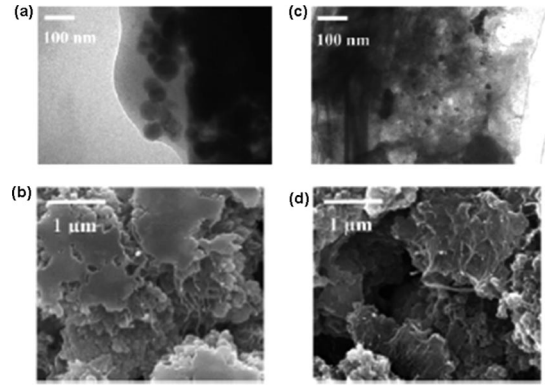


Figure 26. (a) TEM and (b) SEM images of $BaTiO_3$ and (c) TEM and (d) SEM images of TiO_2-isotactic polypropylene nanocomposites prepared by an in situ metallocene polymerization technique. Reprinted with permission from ref 171. Copyright 2007 American Chemical Society.

current and to create a smoother surface. An enhancement in mobility from 0.1 to 0.7 $cm^2\ V^{-1}\ s^{-1}$ in pentacene OFETs was achieved by the addition of the PVP layer.

The surface modification of $BaTiO_3$ nanoparticles (BT) with a phosphonic acid (PEGPA) to fabricate high volume fractions (up to 37 vol %) PEGPA-BT:cross-linked PVP nanocomposites was reported recently by Kim et al. (Figure 27A).[174] The nanocomposite dispersions were deposited by spin-coating, followed by a soft baking at 100 °C for 1 min and thermal curing under vacuum at 160 °C for 72 h to ensure full cross-linking of the PVP. The nanocomposites obtained showed significantly reduced leakage current density as compared to the ones obtained without phosphonic treatment of the nanoparticles (see Figure 27B) due to improved dispersion, and differing dielectric constants were obtained for different particle concentrations ($k = 6$ for 16 vol % BT, $k = 9.6$ for 28 vol % BT, and $k = 14$ for 37 vol % BT). Nevertheless, the authors found that the increasing roughness of the nanocomposite films from nanoparticle loading greatly influences the morphology of the overlying pentacene (Figure 27C) and thus OFET device performance. Optimum devices were obtained by combining high volume fraction nanocomposites with a thin planarization layer of pure PVP, yielding a field-effect mobility of 0.17 $cm^2\ V^{-1}\ s^{-1}$, low threshold voltage of −1.1 V, a small subthreshold slope of 0.3 V/decade, and a large $I_{ON}/I_{OFF} \approx 10^5$.

Recently, Lee et al.[175] studied the optimum loading of TiO_2 nanoparticles by blending different concentrations of polyester-modified TiO_2 nanoparticles (ranging from 0 to 5 vol %) into a polyimide matrix. The best compromise between leakage current, dielectric constant, and pentacene OFET mobility was found for the nanocomposites with 1 and 2 vol % TiO_2. In fact, the authors reported higher mobilities (0.181−0.176 vs 0.119 $cm^2\ V^{-1}\ s^{-1}$) as compared to pure polyimides for these nanocomposites and with comparable I_{ON}/I_{OFF} ratios ($\sim 10^5$), even if the grain size of the pentacene decreased with nanoparticle loading (see Figure 28). This is attributed to more efficient charge transfer through better connected and lower angle grain boundaries.

TiO_2−polymer nanocomposites have also been used to decrease the photosensitivity of organic thin film transistors. Thus, Chuang et al.[176] reported a method to fabricate transparent pentacene-based OFETs with low photosensitivity by introducing blends of TiO_2 with two different polymers, cross-linked PVP and PMMA. In addition to smoothing the surface of the gate insulator, they overcoated the nanocom-

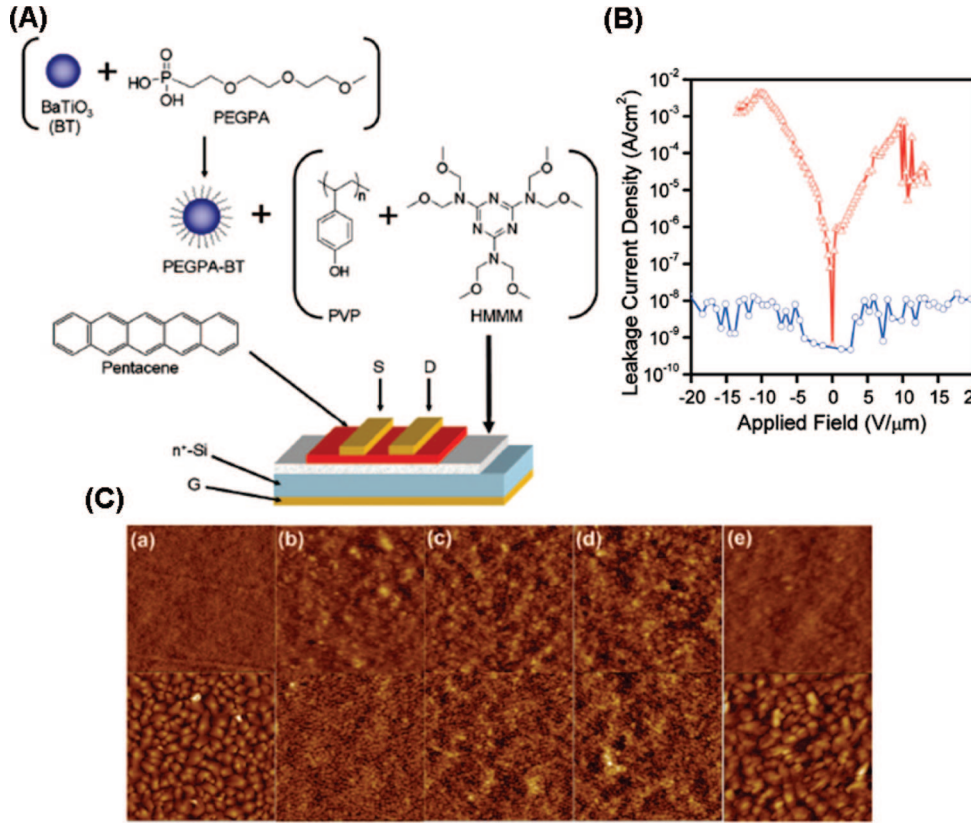


Figure 27. (A) Schematic of PEGPA-BT:PVP nanocomposite preparation and the structure of OFET devices fabricated. (B) Comparison of the leakage current densities of nanocomposite thin films containing 37 vol % of surface-modified BT (○) and unmodified BT (△). (C) AFM height images of gate insulator surfaces (top row) and pentacene layers deposited on each surface (bottom row) for (a) pure PVP, (b)−(d) PEGPA-BT:PVP nanocomposites with 16, 18, and 37 vol % BT, respectively, and (e) 37 vol % PEGPA-BT:PVP nanocomposite with a planarization layer of pure PVP. Image size 5 × 5 μm^2. Reprinted with permission from ref 174. Copyright 2008 American Institute of Physics.

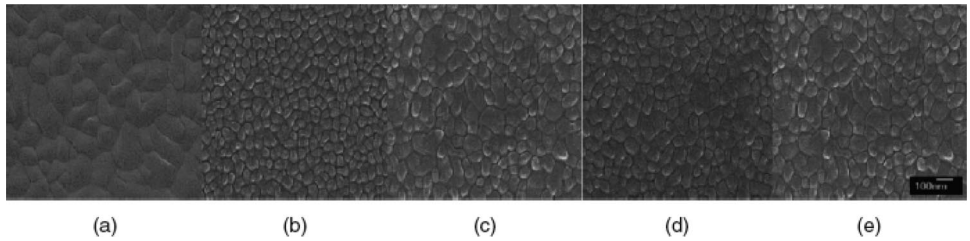


Figure 28. Microstructures of pentacene films deposited on the TiO_2−polyimide nanocomposite insulators having different TiO_2 contents: (a) 0, (b) 1, (c) 2, (d) 3, and (e) 5 vol %. Reprinted with permission from ref 175. Copyright 2008 Japan Society of Applied Physics.

posite layer with a thin layer (∼2 nm) of poly(α-methylstyrene) (PαMS). They observed an increase in the dielectric constant from 4.3 (cross-linked PVP), 2.7 (PMMA) to 4.8, 2.9, respectively, after blending with TiO_2 nanoparticles. As shown in Figure 29, the photosensitivity of the devices was greatly decreased by the introduction of the high-k TiO_2 nanoparticles in both polymer matrices. The authors proposed that the TiO_2 nanoparticles serve as recombination centers (due to the TiO_2 conduction band location between the pentacene HOMO and the LUMO) for excess and trapped electrons, thus reducing electron trapping.

A ceramic-powder polymer composite using a P(VDF-TrFE) 50/50 mol % copolymer as the polymer matrix and $Pb(Mg_{1/3}Nb_{2/3})O_3$−$PbTiO_3$ as the ceramic powder was characterized as a dielectric by Bai et al.[177] They found that, as expected, the dielectric constant increased with the volume fraction of ceramic filler. Furthermore, considering that previous research on P(VDF-TrFE) copolymers indicates that high energy irradiation with proper dosage can increase the room-temperature dielectric constant,[178] they irradiated their composites with the ceramic volume percentages ranging from 10% to 60% at 120 °C. The used a 2.55 MeV electron source with different dosages (40, 60, and 80 Mrad). As shown in Figure 30, for a composite with a 50% ceramic volume content, the dielectric constant is quite high ($k \approx$ 250) and exhibits a weak temperature dependence; however, the mechanical properties are poor. Furthermore, these authors reported that adjusting the dosage of the irradiation allows tuning of the dielectric characteristics.

The same P(VDF-TrFE) copolymer discussed above was recently used by Yildirim et al.[179] to fabricate ferroelectric nanocomposites using barium titanate nanopowders. By increasing the nanopowder loading (from 0 to 50 vol %), the authors obtained flexible films with dielectric constants up to 51.5. Furthermore, these nanocomposites allow the fabrication of low-voltage OFETs with ferroelectric hysteresis and good memory retention. Dang et al.[180] reported a three-component composite composed of $BaTiO_3$ and Ni

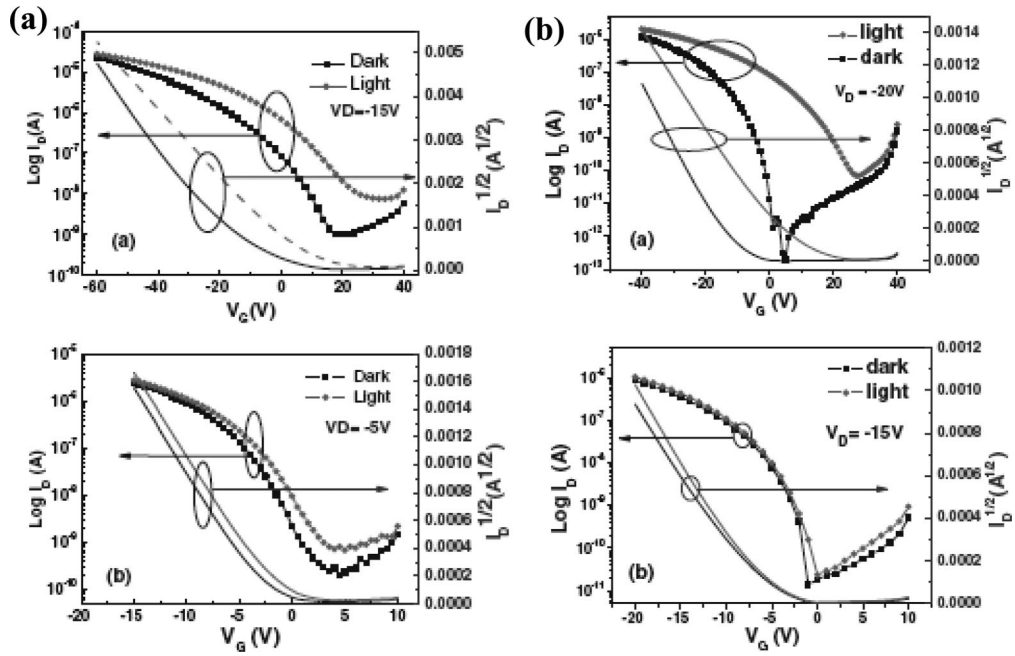


Figure 29. (a) Transfer characteristics of pentacene OFETs in the dark and under illumination, with neat cross-linked PVP as the gate dielectric layer (upper) and with a cross-linked PVP/PαMS bilayer insulator blended with 1 wt % TiO_2 nanoparticles (lower). (b) Transfer curves for devices in the dark and under the light illumination with neat PMMA (upper) and PMMA blended with 1 wt % TiO_2 nanoparticles as the gate insulator (lower). Reprinted with permission from ref 176. Copyright 2007 Japan Society of Applied Physics.

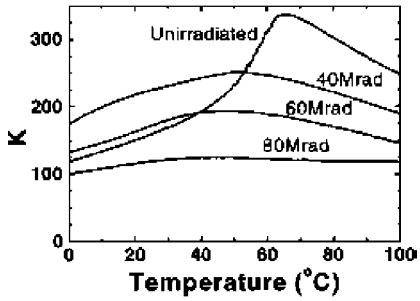


Figure 30. Dielectric constant temperature dependence of P(VDF-TrFE)−$Pb(Mg_{1/3}Nb_{2/3})O_3$−$PbTiO_3$ composites with 50% volume percentage of ceramic filler under different irradiation doses. Reprinted with permission from ref 177. Copyright 2000 American Institute of Physics.

powders in a polyvinylidene fluoride (PVDF) matrix. They compared $BaTiO_3$/PVDF and Ni-$BaTiO_3$/PVDF composites and found that only a small increase in the dielectric constant occurred upon introducing the Ni particles unless the metallic particle concentration was very close to the percolation threshold.[181] In this case, a dielectric constant above 800 was achieved. One of the advantages of these three-phase composites is the combination of easy processability, mechanical flexibility, and good dielectric behavior. In a following paper,[182] another three-component composite was reported, which, instead of Ni particles, incorporated conductive carbon fibers. A dielectric constant of 120 was achieved. The same group also investigated the dielectric behavior of two kinds of Li- and Ti- doped NiO (LTNO)/PVDF composites.[183] They found a remarkable difference in the dielectric constant of the composites having different LTNO fillers, obtaining for one formulation a dielectric constant of ~600.

In 2005, Schroeder et al.[184] reported high-capacitance gate insulators that were processable from aqueous solution. In this case, the nanocomposites were composed of $BaTiO_3$ nanoparticles dispersed in poly(vinyl alcohol) (PVA) or in a PVA random copolymer, poly(vinyl alcohol)-*co*-poly(vinyl acetate)-*co*-poly(itaconic acid) (PVAIA). Both types of nanocomposites exhibit leakage currents below 10^{-5} A cm^{-2} with an electric field of ±2 MV/cm. The dielectric constants for the PVAIA/$BaTiO_3$ insulators ranged between 9 and 12, depending on the density of nanoparticles incorporated in the dielectric. The highest mobility for a pentacene-based device was 0.4 cm^2 V^{-1} s^{-1} for the device using the lowest-*k* dielectric versus 0.12 cm^2 V^{-1} s^{-1} for the highest-*k* one. The authors ascribed this to surface roughness differences. For the $BaTiO_3$/PVA nanocomposite, a dielectric constant of 10.9 and a pentacene mobility of 0.35 cm^2 V^{-1} s^{-1} were measured.

To improve the dispersion of nanoparticles in various polymers, Noh et al.[185] treated Al_2O_3 particles with a *c*-glycidoxypropyl-trimethoxysilane couping agent and then dispersed them in a PVP matrix. In these functionalized nanocomposite dielectrics, the mechanical and electrical stability as well as the surface roughness were significantly improved. In particular, the dielectric constant increased monotonically from 4.9 for pure PVP to 7.2 for the nanocomposite with 24 vol % Al_2O_3. The mobilities measured for pentacene were decreased as compared to the pure PVP dielectric due to greater surface roughness; however, the I_{ON}/I_{OFF} ratio was increased by 3 orders of magnitude (from 10^2 to 10^5). In a more recent paper, Huang et al.[186] investigated the surface treatment of Al nanoparticles with octyl-trimethoxysilane coupling agent dispersed in a linear low density polyethylene (LLDPE) matrix. A comparison between surface-treated and nonsurface treated Al nanoparticles[187] was presented. Because of the self-passivating nature of Al nanoparticles, both the treated and the untreated particles contain an oxide shell around the metallic core that has a dramatic influence on the electrical properties of the composites. The advantages found upon surface treatment are: (i) better dispersion of Al nanoparticles in the LLDPE matrix; (ii) easy control of the dielectric constant; (ii) less dielectric loss in the nanocomposites; (iv) the possibility of

increasing the nanofiller concentration, which translates into an improvement of the mechanical and thermal properties; and (v) stability of the dielectric characteristics with frequency, this being very important for electronic applications.

The polymer PMMA represents a particularly suitable polymer for use as a matrix for high-*k* inorganic fillers. Some examples that are extensively reviewed in the work of Tondello et al.[188] are the following: (i) entrapment of micrometer-sized zinc sulphide powders in PMMA for alternating current powder electroluminiscent lamps; (ii) preparation of low-*k* inorganic−organic hybrid films based on PMMA−PVC blends and a hydrophobic silica powder, functionalized on the surface with trimethylsiloxane groups; and (iii) formation of covalent bonds between a PMMA matrix and embedded zirconium oxoclusters. Table 3 summarizes the dielectric and OFET characteristics of reported polymer−nanoparticle composite gate dielectrics.

3.3.2. Inorganic−Organic Bilayers

Another strategy to combine both inorganic and organic materials advantages in dielectric materials is the fabrication of bilayer inorganic−organic structures. Some of the approaches used so far are presented in this section.

In 2005, Tardy et al.[189] fabricated a new gate dielectric composed of a PMMA/Ta_2O_5 bilayer, where the PMMA was spin-coated on top of an evaporated layer of Ta_2O_5. They analyzed different PMMA thicknesses and found that optimum pentacene device characteristics were achieved when the PMMA thickness was about 37 nm. In comparison to devices with only Ta_2O_5, the operating voltages of these bilayer devices increase to 20−30 V (vs 2.5 V for Ta_2O_5), but the field-effect mobility (0.3 $cm^2\ V^{-1}\ s^{-1}$) and I_{ON}/I_{OFF} ratio ($\sim 10^5$) are increased. In a subsequent paper, Tardy et al. optimized this result and obtained a pentacene mobility of 0.68 $cm^2\ V^{-1}\ s^{-1}$ with an I_{ON}/I_{OFF} of 10^5 when using a PMMA/e-beam evaporated Ta_2O_5 hybrid dielectric.[101] Here, they found that even if pentacene is present in the same morphology, the pentacene growth mode and ordering on PMMA and on the hybrid PMMA/Ta_2O_5 dielectric appear identical; the highest mobility was invariably observed for devices with the bilayer dielectric configuration. This result highlights the advantage of using a bilayer dielectric polymer/high-*k* oxide to improve OFET performance.

PMMA was also used with Al_2O_3 by Park et al.,[190] and they reported that the polymer layer greatly decreases the rms roughness of the metal oxide below 1.51 nm. They controlled the roughness by changing the thickness of the polymer layer; however, they found that it had little effect on the measured pentacene carrier mobility, in contrast to what it is usually found for inorganic dielectrics. Furthermore, the low surface energies of the PMMA/Al_2O_3 gate dielectrics reduce the wetting of pentacene and minimize the interaction between the pentacene and the gate dielectric layer surface. Another type of high-capacitance bilayer dielectric based on atomic-layer-deposited HfO_2 and spin-coated epoxy was fabricated by Rogers et al. for SWCNT devices.[191] These hybrid insulators exhibited desirable dielectric properties with capacitances as large as 330 nF cm^{-2} and low leakage currents ($\sim 10^{-8}$ A cm^{-2}). These dielectrics can be deposited both on Si and on flexible ITO/PET substrates. Both p−n SWCNT devices and complementary logic gates were fabricated on these flexible substrates with low hysteresis and low operating voltages. The mechanical robustness of the devices was also demonstrated in bending tests up to 1%, with the bendability achieved sufficient for some applications in flexible electronics.

Low hysteresis pentacene-based OFETs were also fabricated using a bilayer dielectric composed of plasma-enhanced chemical vapor-deposited SiO_2 and cross-linked PVA.[192] The lowest hysteresis was found for a device with 350 Å of SiO_2 and 950 Å of PVA. The authors argued that in these double-layer dielectric devices, the SiO_2 layer blocks charge injection from the gate electrode to the cross-linked PVA bulk or interface, thereby reducing the hysteresis. Furthermore, the pentacene field-effect mobility (0.12 $cm^2\ V^{-1}\ s^{-1}$) was enhanced as compared to that on bare SiO_2 due to the high-*k* characteristics of the cross-linked PVA. The I_{ON}/I_{OFF} ratio was also high ($\sim 2 \times 10^6$) due to the reliable leakage characteristics of the SiO_2 layer. The stability of these devices was also improved by the double-gate dielectric. In 2006, Im et al.[193] fabricated polymer/YO_x hybrid-sandwich gate dielectrics and used them in semitransparent pentacene-based OFETs. Using different double-layer dielectrics, PVP(45 nm)/YO_x(100 nm) and PVP(70 nm)/YO_x(100 nm), they improved device operation. The insulators studied here combined good dielectric characteristics (capacitances of 47.1 and 35.2 nF cm^{-2}, respectively, leakage currents of ca. 10^{-6} $cm^2\ V^{-1}\ s^{-1}$, and dielectric strength of 2 MV cm^{-1}) and improved surface smoothness. Field-effect mobilities of 0.83 and 0.40 $cm^2\ V^{-1}\ s^{-1}$ in a voltage range of −5 V and threshold voltages of about −1 V were measured for the thin and thick double gate dielectrics, respectively. One of the advantages of the PVP polymer in contrast to PMMA is its cross-linking properties, which allows deposition of the semiconductor layer by solution processes without damaging the dielectric layer. To this end, Cao et al.[194] fabricated a solution-processed P3HT device using a double layer dielectric composed of anodized Ta_2O_5 (120 nm) and cross-linked PVP (250 nm) with a capacitance of 11.6 nF cm^{-2} and compared it to the single layer dielectric devices using Ta_2O_5 (600 nm and $C = 184$ nF cm^{-2}) or PVP (600 nm and $C = 5.16$ nF cm^{-2}). These authors reported that OFETs with a PVP layer covering the metal oxide dielectric could effectively increase the mobility from $\sim 10^{-3}$ to 3×10^{-2} $cm^2\ V^{-1}\ s^{-1}$ while maintaining the same low threshold voltage (1.7 V) of the single dielectric layer Ta_2O_5 devices and decreasing the leakage current.

The same bilayer dielectric structure was also used by Zhao et al.[64b] to demonstrate improved photostability in pentacene-based devices. The better performance was attributed to the low trap density and high photostability of the PVP polymer versus the charge trapping effects present in Ta_2O_5 dielectric layers (see Figure 31). An enhancement of mobility from 0.32 (Ta_2O_5)−0.34 (PVP) $cm^2\ V^{-1}\ s^{-1}$ to 0.46−0.48 $cm^2\ V^{-1}\ s^{-1}$ in the bilayer structure was found without alteration of the I_{ON}/I_{OFF} ratio. The optimum photostability was exhibited by a Ta_2O_5 (100 nm)/PVP (50 nm)-based device, where the variation of the threshold voltage upon illumination was found to be only 0.04 V (Figure 31). A higher mobility of 0.66 $cm^2\ V^{-1}\ s^{-1}$ for pentacene was achieved by Chu et al.[195] using a hybrid PVP-capped MgO dielectric. The capacitance of the MgO/PVP hybrid bilayer (35.7 nF cm^{-2}) was found to be greater than that for PVP alone. Furthermore, the PVP layer reduced the leakage current and smoothed the dielectric surface, optimizing pentacene morphology. This resulted in a pentacene polycrystalline structure having several domain sizes.

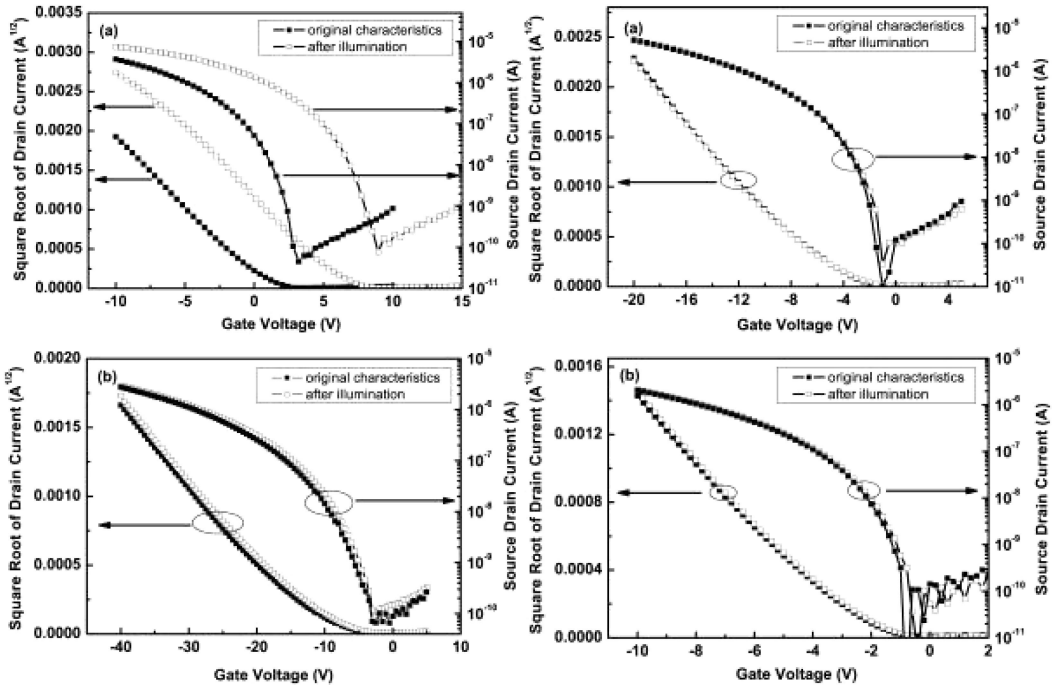


Figure 31. Left: Transfer curves and plots of $I_D^{1/2}$ vs V_G for pentacene-based OFETs with (top) a 300 nm Ta_2O_5 insulator at $V_D = -10$ V and with (bottom) a 500 nm PVP insulator at $V_D = -40$ V. Right: Transfer curves and plots of $I_D^{1/2}$ vs V_G for pentacene-based OFETs with (top) a Ta_2O_5-234 nm/PVP-66 nm insulator at $V_D = -20$ V and (bottom) a Ta_2O_5-100 nm/PVP-500 nm insulator at $V_D = -10$ V. Reprinted with permission from ref 64b. Copyright 2007 American Institute of Physics.

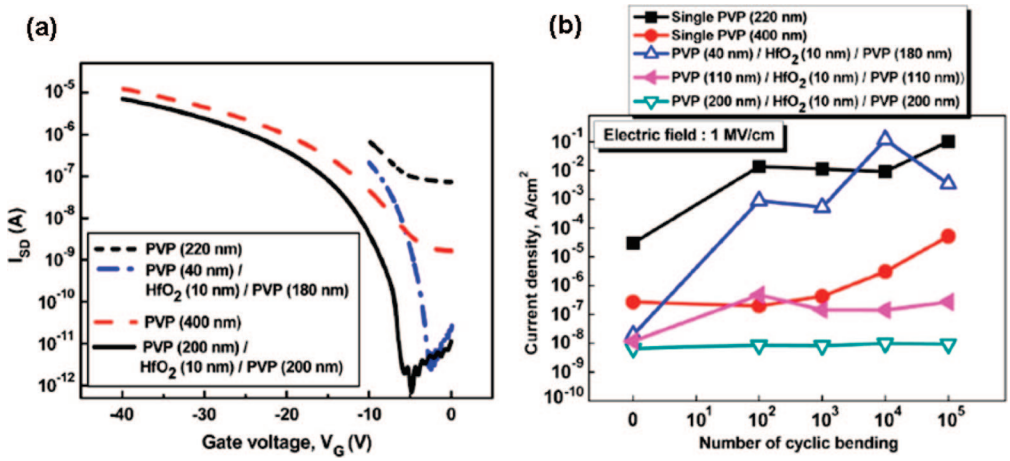


Figure 32. (a) Transfer characteristics of pentacene-OFETs with various PVP and HfO_2 dielectric stacks. Transfer characteristics of the OFETs with total thicknesses of 220 and 400 nm were measured at $V_D = -10$ and -40 V, respectively. (b) Leakage current density of the different gate dielectric stacks as a function of bending cycles at the electric field of 1 MV/cm and a frequency of 100 kHz. Reprinted with permission from ref 196. Copyright 2008 American Institute of Physics.

Trilayer PVP/HfO_2/PVP dielectric stacks have been also used in flexible pentacene devices.[196] In this case, incorporation of an ultrathin, atomic layer deposition grown HfO_2 layer between two PVP organic layers greatly reduces the leakage current, and consequently increases the I_{ON}/I_{OFF} ratio without degrading the mechanical flexibility of the devices. Mobilities up to 0.56 $cm^2\ V^{-1}\ s^{-1}$, V_T of -17 V, and $I_{ON}/I_{OFF} \approx 10^6$ were measured for PVP (200 nm)/HfO_2 (10 nm)/PVP (200 nm) dielectric-based devices (Figura 32a). Furthermore, the authors reported that the use of a top PVP layer having 200 nm thickness greatly decreased the strain on the inorganic HfO_2 layer, with the leakage current remaining unaltered after 10^5 bending cycles (see Figure 32b).

Another approach to improve HfO_2 dielectric layers for pentacene-based devices has been reported by Jen et al., by the functionalization of the sol−gel-derived HfO_2 surfaces with various anthryl-terminated alkyl phosphonic acid SAMs and with ODPA (Figure 33).[197] The authors demonstrated that $\pi-\sigma$ phosphonic acid-based SAM/HfO_2 hybrid dielectrics combine the strengths of molecular SAMs with high-k metal oxides while providing a chemically and electrically compatible pentacene/dielectric interface.

These hybrid dielectrics exhibited high capacitances (ranging from 580 to 690 nF cm^{-2}) and low leakage currents of $\sim 10^{-9}$ A cm^{-2} at applied voltages of -1.5 V (see Figure 33d). A field-effect mobility of 0.22 $cm^2\ V^{-1}\ s^{-1}$ was recorded for the $\pi-\sigma$-PA1/HfO_2 dielectric with an $I_{ON}/I_{OFF} \approx 10^5$ and $V_T = -0.41$ V. The highest mobility of this dielectric as compared to $\pi-\sigma$-PA2/HfO_2 and ODPA suggests that the chemical compatibility at the pentacene/dielectric interface is affected not only by the surface group but also by its orientation. In a following paper, the

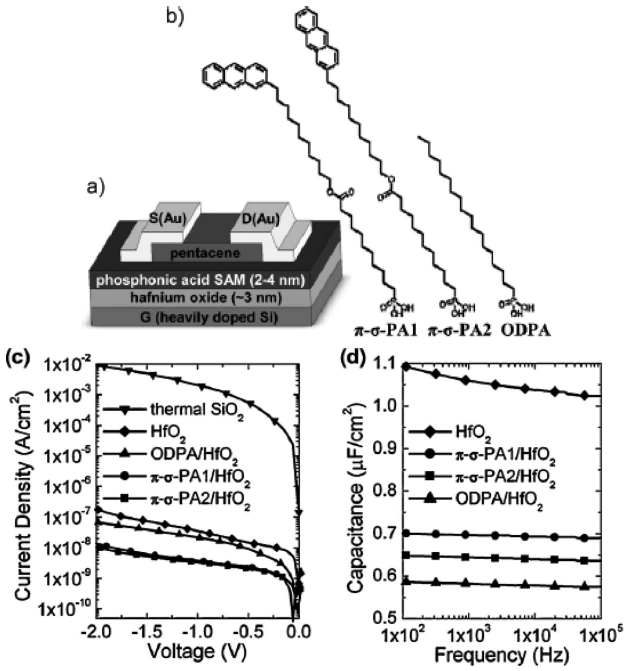


Figure 33. (a) Schematic view of a top contact OFET using different SAM/HfO_2 hybrid gate dielectrics. (b) Structures of the phosphonic acid SAMs used in the fabrication of the devices. (c) Leakage current density versus applied voltage and (d) capacitance versus frequency of the different hybrid dielectrics. Reproduced with permission from ref 197. Copyright 2008 Wiley−VCH Verlag CmbH & Co. KGaA.

compatibility of the ODPA SAM/HfO_2 dielectric with n-type semiconductors was demonstrated by the fabrication of C_{60}-based devices.[198] The corresponding C_{60}-OFETs exhibited good figures of merit: $\mu = 0.28$ cm^2 V^{-1} s^{-1}, $V_T = 0.35$ V, subthreshold slope of 100 mV/dec, and $I_{ON}/I_{OFF} \approx 10^5$, indicating an enhanced device performance as compared to bare HfO_2 due to a more compatible semiconductor/dielectric interface.

One example that clearly shows the importance of the dielectric−semiconductor and metal contact−semiconductor interfaces was reported by Kippelen et al.[199] In their work, high-performance C_{60}-based OFETs with average mobilities of 2.5 cm^2 V^{-1} s^{-1} at gate voltages below 5 V were fabricated, using Ca source and drain electrodes, and atomic layer-deposited Al_2O_3, modified with divinyltetramethyldisiloxane-bis(benzocyclobutene) (BCB), as the dielectric layer. The addition of the BCB layers provides a high-quality hydroxyl-free interface, a leakage current below 10^{-8} A cm^{-2}, and high dielectric strength exceeding 3 MV/cm, with a total capacitance of the 50 nF cm^{-2}. Furthermore, the authors report that the combination of Ca source and drain electrodes and a bilayer dielectric not only enhances device performance but also greatly improves both the electrical stability and the reproducibility.

The first example of a polymeric semiconductor-based OFET fabricated with a solution processable TiO_2−polymer gate dielectric at low temperature was reported by Liu et al. in 2008.[200] In this bilayer dielectric, the polymer smoothes the TiO_2 surface and suppresses the leakage current from the grain boundaries of the TiO_2 films. For additional treatment of the dielectric interface, Lui et al. introduced a SAM modification (HMDS or OTS) before the spin deposition of the P3HT semiconductor. The resulting solution-processed OFETs could operate at voltages below 10 V and showed a field-effect mobility of 0.0140 cm^2 V^{-1} s^{-1}, a threshold voltage of 1.14 V, and $I_{ON}/I_{OFF} \approx 10^3$.

Majewski et al.[104] reported two different modifications of anodized Ti dielectric layers. In a first paper, the anodized-Ti/TiO_2 surface was capped with an ultrathin layer of poly(α-methylstyrene) (PAMS), decreasing the leakage current by 2 orders of magnitude (Figure 34a). Using this hybrid dielectric ($C = 228$ nF cm^{-2}), high-quality pentacene OFETs with exceptionally low leakage and relatively high performance ($\mu = 0.8$ cm^2 V^{-1} s^{-1}), functioning below 1 V, were fabricated (Figure 34b). In a second paper, Majewski et al. treated the TiO_2 with a monolayer of OTS ($C = 465$ nF cm^{-2}) and found good performance for both pentacene and poly(triarylamine) (PTAA) OFET devices.[105] With the OTS treatment, the thickness of the dielectric could be reduced, because leakage currents were suppressed, and field-effect mobilities of 0.25 cm^2 V^{-1} s^{-1} were obtained for pentacene, as compared to 0.12 cm^2 V^{-1} s^{-1} for the untreated TiO_2 layer (in a voltage range of 1 V).

Organic−inorganic 22 nm thick hybrid dielectrics (AlO_x-SAM-based single layers and AlO_x/TiO_x/AlO_x-SAM-based trilayers) were used to fabricate ZnO field-effect transistors.[201] These dielectrics exhibit high capacitances, 130 and 220 nF cm^{-2} for the AlO_x-based single layer and for the

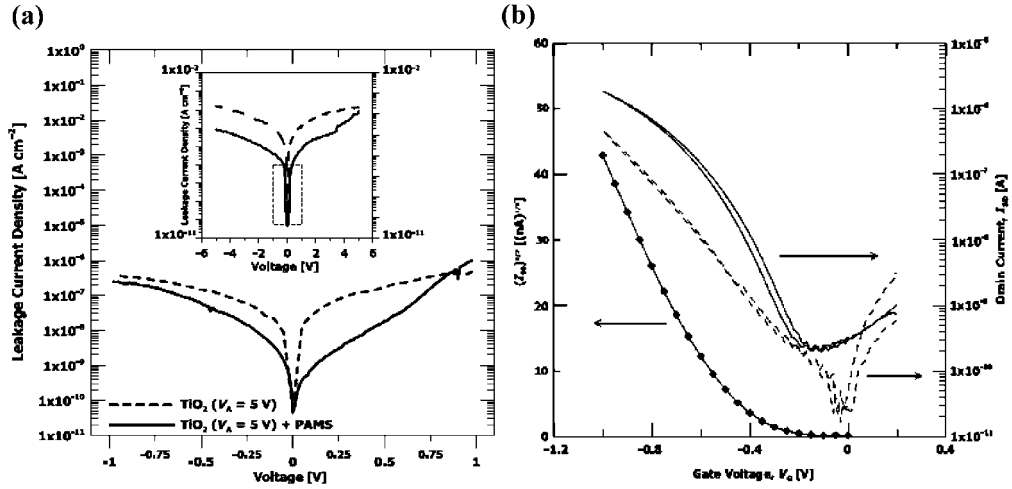


Figure 34. (a) Leakage behavior of anodized TiO_2 films. Dashed line: bare oxide anodized at $V = 5$ V. Solid line: after capping with poly(α-methylstyrene). (b) Transfer characteristics of the pentacene-OFET (solid line) and the leakage current (dashed line). $I_D^{1/2}$ vs V_G is also presented in the graph (◆). Reprinted with permission from ref 104. Copyright 2005 Wiley−VCH Verlag CmbH & Co. KGaA.

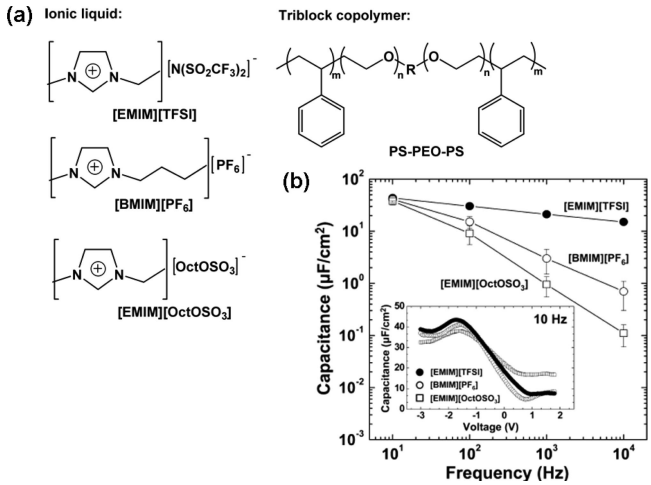


Figure 35. (a) Chemical structures of the ionic liquid and triblock copolymer ion gel components. (b) Frequency dependence of the maximum capacitance for the three different ion gels. Inset shows $C-V$ characteristics at 10 Hz. Reprinted with permission from ref 203b. Copyright 2008 Wiley−VCH Verlag CmbH & Co. KGaA.

trilayer, respectively. The trilayer dielectric-based devices exhibit superior performance (mobility of 0.66 $cm^2\ V^{-1}\ s^{-1}$ versus 0.36 $cm^2\ V^{-1}\ s^{-1}$ for the single layer dielectric) but were less stable and could not be operated at voltages above 2 V due to lower dielectric strength of the TiO_x-based layer. The devices also exhibited little gate hysteresis, indicating that the nanohybrid dielectric approach may be appropriate for achieving electrically stable ZnO-FETs operating at low voltages.

Table 4 summarizes the dielectric and OFET characteristics of various inorganic−organic bilayer gate dielectrics.

3.3.3. Hybrid Solid Polymer Electrolytes

A different class of hybrid gate dielectric that has been recently reported is the solid-state polymer electrolyte. This alternative strategy consists principally of a Li^+ salt dissolved in poly(ethylene oxide) (PEO). Using this $LiClO_4$/PEO dielectric, low-voltage transistors have been fabricated using various semiconductors.[202] The principal drawback of these dielectrics is that the speed of the devices is determined by the polarization response time of the polymer electrolyte. To solve this problem, Frisbie et al.[203] fabricated high-capacitance ion gel gate dielectrics that have a significant faster response. These ion gels comprise a polymer network (PS-PEO-PS) swollen with different ionic liquids (Figure 35a). They show capacitances up to 40 $\mu F\ cm^{-2}$, comparable to reported SAMs or thin ceramic high-k gate insulators.[36g] The authors indicate that these large capacitances are associated with the formation of nanometer-thick electrical double layers at the electrode−electrolyte interfaces. In their first publications, using P3HT as the semiconductor, high capacitance ion gel-gated transistors with average mobilities of ~1 $cm^2\ V^{-1}\ s^{-1}$ and response times of less than 1 ms were fabricated on rigid substrates using conventional shadow-masking and spin-coating techniques (Figure 35). In a following paper, these authors assessed the broad utility of these ion-gels as gate dielectrics by testing them with three different p-channel polymer semiconductors: P3HT, poly(3,3‴-didodecylquaterthiophene (PQT-12), and poly(9,9′-dioctylfluorene-co-bithiophene) (F8T2).[204] Frisbie et al. obtained hole mobilities of 1.8, 1.6, and 0.8 $cm^2\ V^{-1}\ s^{-1}$, respectively, higher than previously reported for the same semiconductors.[103,205] In this paper, the compatibility of these ion-gels with printing methods was also demonstrated, using an aerosol jet printing method to fabricate an array of GEL-OFETs and resistor-loaded GEL-OFET inverters on flexible polyimide substrates (see Figure 36). In this case, they used PS-PMMA-PS instead of water-soluble PS-PEO-PS to avoid dissolution of the gel layer during the fabrication process. The devices exhibited good reproducibility and remarkable stability; nonetheless, they exhibit the disadvantage of high "off" currents (~10 nA). Interestingly, the authors demonstrated that the high polarizability of the ion gels also enables the gate electrodes to be physically offset from the source and drain channel, which is interesting for future printing-based applications.

4. Summary

From the analysis of recent advances in OFETs, it becomes clear that developing new low-cost technologies requires replacement of the traditional dielectric materials commonly used for inorganic/Si transistor and capacitor fabrication. While using thermally grown SiO_2 as gate dielectric affords mobilities competing with that of amorphous silicon, such dielectrics have the drawback of high operating voltages,

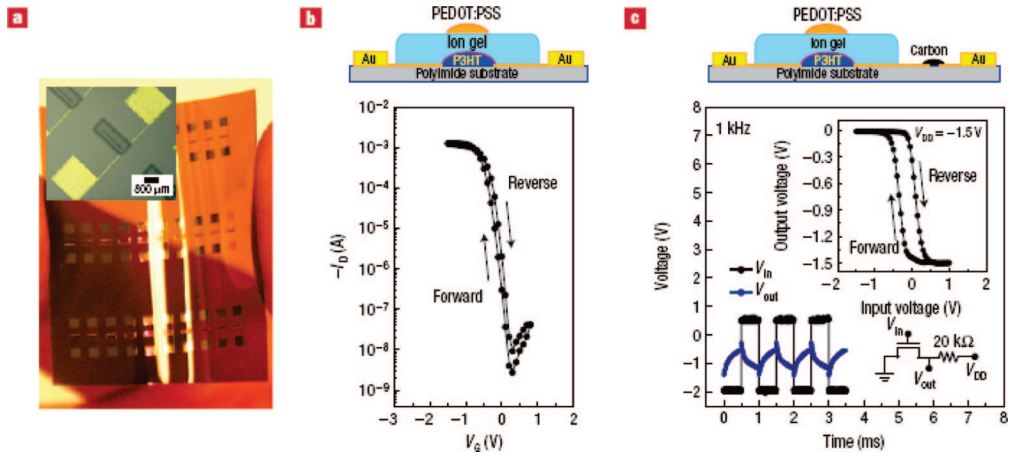


Figure 36. (a) Optical image of an aerosol-printed GET-OFET array fabricated on a flexible polyimide substrate. (b) Schematic diagram and transfer characteristics of a P3HT-based GEL-OFET at $V_D = -1$ V. (c) Schematic diagram and output voltage response of a resistor loaded GEL-OFET inverter at $V_D = -1.5$ V when V_G is pulsed at 1 kHz. The input−output voltage characteristics are shown in the inset. Reprinted with permission from ref 204. Copyright 2008 Macmillan Publishers Ltd.

implying high power dissipation, which is impractical for mobile devices. Decreasing the SiO_2 thickness can lead to higher capacitances, but for ultrathin layers high leakage currents dominate the device performance. The first approach to increase capacitance in organic devices was to replace SiO_2 with high-*k* metal oxides because this approach is widely used in inorganic electronics. Principal limitations that this first option presents are processability, mechanical flexibility, and compatibility of these inorganic dielectrics with organic semiconductors. Although most metal oxides are deposited using vacuum techniques, several solution-based methodologies are possible such as wet-anodization and chemical bath deposition. However, these materials must usually be surface-modified to enhance semiconductor film growth. Furthermore, their poor mechanical properties limit their use in flexible electronics. An option to overcome the limitations of metal oxide dielectrics is to employ polymer dielectrics. This option has led to the fabrication of all-printed flexible organic devices; however, the polymers typically have low dielectric constants as compared to metal oxides, and they usually require large thicknesses as gate dielectrics to avoid high leakage currents. The last issue has been addressed by using cross-linked polymers, in this case making possible the fabrication of thin polymer gate dielectrics meeting the requirements for electronic devices. Furthermore, cross-linking of the polymer insulators enables the deposition of the subsequent layers by solution-based processes, without dissolving/swelling the underlying gate dielectric layer. Self-assembled monolayers and multilayers also offer great promise for organic electronics. These low-leakage nanodielectrics have allowed the fabrication of very thin gate dielectrics, which translate into higher capacitances, and enhance the performance of both organic and inorganic FETs.

More recently, to combine the desirable properties of high-*k* metal oxides and polymeric dielectric processability and mechanical flexibility, a new approach for fabricating gate dielectrics has emerged. Here, hybrid inorganic−organic dielectrics have been used, either by dispersion of inorganic nanoparticles in a polymer matrix or by stacking inorganic−organic bilayers. The principal limitation of the former is to obtain a good dispersion of the nanoparticles in the matrix; however, several approaches have been used to improve the dispersion. On the other hand, the use of stacked inorganic−organic layers offers a good option because it overcomes the drawback of the poor compatibility of most metal oxides with organic semiconductors and usually reduces the roughness of the dielectric layer. Finally, the use of hybrid solid polymer electrolytes has appeared as a feasible option to increase capacitance due to the formation of an electrical double layer at the electrode−electrolyte interface. Furthermore, because of their high polarizabilities, they offer the flexibility of locating the gate electrode in such a way that it is not directly aligned with the semiconductor channel.

5. Acknowledgments

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